CROSSTALK NOISE REDUCTION USING DRIVER SIZING OPTIMIZATION IN VLSI RC GLOBAL INTERCONNECTS USING 90NM PROCESS TECHNOLOGY

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ABSTRACT
In this paper noise avoidance in closed form crosstalk noise model for on-chip VLSI RC interconnects using $2\pi$ model is presented. In this crosstalk noise model we consider the case when step input is applied to the aggressor which is adjacent to the victim net and further simplified it, then find out the closed form formulae for noise pulse width and noise amplitude for RC interconnect. Various noise avoidance approaches can be used for crosstalk noise reduction. This paper presents crosstalk noise reduction using driver sizing optimization. Sensitivity expressions of driver resistance to peak noise and noise width are used in this work.

Keywords- Noise Modelling, Crosstalk, On-Chip RC Interconnect, Step Input, VLSI.

I. INTRODUCTION
Due to the advancement in VLSI technology feature size is reduced which affects the crosstalk noise problem and also affects the design’s timing and functionality goals [1-2]. As a result of this chip area is reduced which degrades the performance of VLSI circuits such as logic failure, unwanted coupling voltage between two adjacent wires, timing delay etc. Decreasing feature size also increases crosstalk noise which is produced due to the parasitic coupling between interconnects. The amount of this crosstalk noise can be calculated by using circuit and layout techniques [3]. Coupling capacitance is high; it is the sum of area capacitance and the fringing capacitances of a wire. According to the trends, the role of this coupling capacitance will be more dominant in the future as feature sizes shrink. Due to this coupling capacitance crosstalk noise is induced in the circuit, which reduces the performance and reliability of the circuit. This may also induce unwanted voltage spikes in neighboring nets. An aggressor net is physically adjacent to a victim net and may be modeled as being connected with the help of a distributed coupling capacitance.

In the current technology, noise analysis and avoidance are becoming equally important or in some cases, more important than the timing and power analysis. Crosstalk noise exhibits a negative impact on the reliability of the VLSI circuits. In these circuits, it is very common to have wires running adjacent to another known as aggressor and victim nets. The net on which noise is being induced is called the victim net; whereas, the net that induces this noise is called the aggressor net. In deep submicron design, the parasitic coupling effects become significant due to the greater proximity of adjacent wires and the increase in the switching speeds of the signals. Hence it has become necessary to consider the crosstalk between parallel RC interconnects lines [4]. Crosstalk is a well-known phenomenon in integrated circuit design. Crosstalk noise may cause various undesirable effects such as overshooting, undershooting, glitches, increasing and reducing a signal delay. In [5-6] various telegraph equations are directly solved and an analytical formula for peak noise in capacitively coupled bus lines is obtained. The work in [7] derives bounds for crosstalk noise using a lumped RC model, but it assumes a step input for aggressor. Extensions to [7] are made in [8-10] to consider a saturated ramp input and $\pi$-circuit to represent the distributed nature of on-chip VLSI interconnect. But most of these models fail to represent the distributed nature of an RC network. The model proposed in [11] considers an Elmore delay like peak noise model for general RC trees but it assumed an infinite ramp input. The peak noise obtained in [11] may even be larger than the supply voltage. Devgan’s metric
has been improved in [12]. One recent work shown in [10] is capable to handle distributed RC network and saturated ramp input. In [13-14], an improved 2-π model is introduced which considers the coupling location at victim net and distributed RC characteristics for victim net. In [15] a improved 2-π model of ramp input for crosstalk noise in time domain is derived then various noise reduction techniques are explained. This paper presents idea about crosstalk noise reduction using sensitivity expressions to driver resistance. This technique is known as driver sizing. Some crosstalk reduction techniques are also discussed in [16-19] for RC VLSI Interconnections.

Remaining part of the paper is synchronized as follows: section 2 describe proposed crosstalk noise model, noise avoidance technique using driver sizing is described in section 3. Section 4 illustrates the simulation results and finally section 5 concludes this paper.

II. PROPOSED CROSSTALK NOISE MODEL

In this section, we first present the 2-π model approach and derive its analytical time-domain waveform when unit step input is applied at the aggressor net. Then we will calculate expressions for peak noise (amplitude) and noise width. The noise avoidance technique known as driver sizing is presented with the help of various sensitivity expressions.

A. 2-π MODEL AND ITS ANALYTICAL WAVEFORM

For explaining the crosstalk noise model, the 2-π model is explained first. In this explanation, victim net is a RC interconnection line. An aggressor line is placed near the victim net, as shown in Figure 1(a) and unit step input voltage pulse is applied at the coupling location on aggressor net. In Figure 1(a), L_s represents the interconnect length of victim net before the coupling. Similarly, L_c and L_e represent the interconnect length of victim net at the coupling and after the coupling, respectively. 2-π model is reduced to a 2-π type RC model as shown in Figure 1(b). This reduction of 2-π model is very useful while calculating the value of crosstalk noise at the receiver end. This model contains two π type RC circuits, known as 2-π model. One RC circuit is located before the coupling and the other is after the coupling. The victim driver is modelled by an effective resistance R_d and other RC parameters are C_X, C_1, R_s, C_2, R_e and C_L. The values of these parameters are computed from the geometric information from Figure 1(b) in the following manner:

The node 2 is known as coupling node; this is set to be the centre of the coupling portion of the victim net i.e. (L_s+L_c)/2 from the source. Let the upstream and downstream interconnect resistance/capacitance at node 2 be R_s/C_s and R_e/C_e, respectively. Then capacitance values are set to be C_1 = C_s/2, C_2 = (C_s+C_e)/2 and C_L = C_e/2+C_1. In some cases one lumped RC for the victim net can be used, but 2-π model can model the coarse distributed RC characteristics. The resulting 2-π model can be solved analytically.

From Figure 1(b), the impedance at node 1, Z_1 satisfying the following,

\[ \frac{1}{Z_1} = \frac{1}{R_s} + sC_1 \]  

Then at node 2, we have

\[ \frac{1}{Z_2} = \left( \frac{1}{Z_1} + R_s \right) + sC_1 + \frac{1}{R_e + sC_e} \]  

V_2(s) denotes the s-domain voltage at node 2, then

\[ V_2(s) = \frac{Z_2}{Z_1} V_{agg}(s) \]  

The output voltage V_{out} in the s-domain is

\[ V_{out}(s) = \frac{1}{R_e + sC_e} \frac{Z_2}{Z_1} V_{agg}(s) \]  

Substituting Z_1, Z_2, and V_2 into V_{out}(s) yields,

\[ V_{out}(s) = \frac{a_2 s^2 + a_1 s}{s^2 + b_2 s^2 + b_1 s + b_0} \]  

where the co-efficients are
The transfer function \( H(s) \) can be expressed into the poles/residues form as,

\[
H(s) = \frac{a_3s^3 + a_2s^2 + a_1s + a_0}{s^3 + b_3s^2 + b_2s + b_1} = \frac{k_1}{s - s_1} + \frac{k_2}{s - s_2} + \frac{k_3}{s - s_3}
\]

(7)

The three poles \( s_1, s_2 \) and \( s_3 \) are the three roots of \( s^3 + b_3s^2 + b_2s + b_1 = 0 \), which can be obtained analytically using standard mathematical techniques. The time domain function of each pole/residue is

\[
V_{\text{out}}(t) = k_ie^{s_i}t
\]

where \( i=1, 2, 3 \)  \hspace{1cm} (8)

For the aggressor with unit step input with normalized \( V_{\text{agg}}=1 \), i.e.

\[
V_{\text{agg}}(s) = \frac{1}{s}
\]

(9)

its Laplace transform is,

\[
V_{\text{agg}}(s) = \frac{1}{s}
\]

(10)

Then for each pole/residue pair, the s-domain output is given by,

\[
V_{\text{out}}(s) = \frac{k_i}{s - s_i}V_{\text{agg}}(s)
\]

(11)

From (3) and (4),

\[
V_{\text{out}}(s) = \frac{k_i}{s - s_i} \left( s - s_i \right) = \frac{k_i}{s - s_i} \left( s_i - s \right)
\]

\[k_i = C_iR_iC_j
\]

\[K = R_jR_iC_jC_i + C_jR_iC_i + C_jR_iC_i + C_iR_iC_j
\]

(12)

So, the time domain expression of the output voltage is

\[
v_{\text{out}}(t) = \frac{k_i}{s_i} \left( 1 - e^{-s_i}t \right)
\]

(13)

Therefore, the final noise voltage is simply the summation of the voltage waveform from each pole/residue pair.

\[
v_{\text{out}}(t) = v_{\text{out1}}(t) + v_{\text{out2}}(t) + v_{\text{out3}}(t)
\]

(14)

Equation (14) gives the final noise voltage waveform. The \( 2\pi \) model has been tested extensively and its waveform from (14) can be shown to be almost identical compared to HSPICE simulations.

**B. CLOSED FORM NOISE AMPLITUDE AND WIDTH**

In this subsection, formulae for noise amplitude and noise width are obtained. This is achieved when we will further simplify the original \( 2\pi \) model.

1) **NOISE AMPLITUDE CALCULATION**

On simplifying equation (2) using dominant-pole approximation method,

\[
v_{\text{out}}(s) = \frac{as}{b_s + b_0}
\]

where \( V_{\text{agg}}(s) = \frac{1}{s} \)

(15)

\[
V_{\text{agg}}(s) = \frac{1}{s}
\]

(16)

So,

\[
v_{\text{out}}(s) = \frac{1}{s}
\]

(17)

where the co-efficient are,

\[
t_s = (R_j + R_i)C_i
\]

(18)

\[
t_t = (R_j + R_i)(C_j + C_i) + (R_iC_j + s_iC_i)
\]

(19)

The term \( t_s \) represents the RC delay term from the upstream resistance of the coupling element times the coupling capacitance. The term \( t_t \) represents distributed Elmore delay of victim net.

The output voltage shown in (6) can be expressed in time domain and given in (20).

\[
v_{\text{out}}(t) = \frac{1}{s} \left( 1 - e^{-t/t_s} \right)
\]

(20)

where \( t \geq 0 \).

From the noise expression shown in (20), it is evident that noise monotonically decreases as \( t \geq 0 \). The value of noise will be maximum at \( t=0 \). This maximum value of noise can be calculated by putting \( t=0 \) in (20).

So,

\[
v_{\text{max}} = \frac{1}{t_s}
\]

(21)

Equation (21) represents the maximum amplitude of noise which is obtained at \( t=0 \).

2) **NOISE WIDTH CALCULATION**

The noise width for a noise pulse is defined to be the length of time interval so that the noise spike voltage \( V \) is larger than or equal to \( V_{\text{agg}} \) where \( V_{\text{agg}} \) represents the threshold voltage.

From (20),

\[
v_{\text{out}}(t) = \frac{1}{t_s} \left( 1 - e^{-t/t_s} \right)
\]

(22)

So,

\[
v_{\text{max}} = \frac{1}{t_s}
\]

(23)

Noise width is the width of time interval between \( t_1 \) and \( t_2 \).
The value of \( t_2 \) can be calculated using equation (23). Hence, \( t_2 \) can be derived as,

\[
  t_2 = t_1 \ln \frac{1}{v_{t2}} \frac{t_1}{v_{t1}}
\]

(24)

At \( t_2 \), the noise voltage is \( v_t \). So,

\[
  t_2 = t_1 \ln \frac{1}{v_{t2}} \frac{t_1}{v_{t1}}
\]

(25)

Noise width is given by,

\[
  t_{width} = t_2 - t_1
\]

(26)

Substituting the values of \( t_1 \) and \( t_2 \) from equations (24) and (25)

t_{width} = t_1 \ln \frac{1}{v_t} \frac{t_1}{v_t}

(27)

In this paper, we assume the value of threshold voltage \( v_t \) to be half of the value of the peak noise voltage \( v_{max} \).

\[
  v_t = \frac{v_{max}}{2}
\]

(28)

From (21), (27) and (28),

\[
  t_{width} = t_1 \ln 2
\]

(29)

This expression represents the width of the noise voltage waveform.

Note that when the time increases beyond \( t_2 \), the noise voltage becomes very less. In the above calculation we ignored the effect of that noise. In some conditions peak noise exceeds certain threshold voltage but remains immune to the noise. This can be expressed clearly by some noise amplitude versus noise width plots.

### III. Noise Avoidance Technique using Driver Sizing

Driver sizing can help to reduce the peak crosstalk noise, since a strong driver is more capable to sustain a noise spike. Our model does indicate some situation under which increasing driver size (i.e., reduce \( R_d \)) may help to reduce the peak noise and noise width. It also indicates the situation under which increasing driver size may not help to reduce the peak noise and noise width. If we consider the case where the aggressor driver is sized down, its effective conductance decreases thus as a result of this it induces less amount of noise on a victim net driver. This can be explained with the help of sensitivity expressions of peak noise and noise width to driver resistance \( R_d \).

\[
  \frac{\partial v_{max}}{\partial R_d} = \frac{C_s}{t_1} \left( \frac{t_1}{t_0} (c_1 + c_2 + c_3) \right)
\]

(30)

\[
  \frac{\partial t_{width}}{\partial R_d} = \frac{C_s}{t_1} \left( \ln \left( \frac{1}{v_t} \frac{t_1}{t_0} \right) - 1 \right) (c_1 + c_2 + c_3)
\]

(31)

These above sensitivity expressions discuss the effect of the driver resistor size on the maximum noise amplitude and noise width in the RC interconnection lines.

### IV. Simulation Result and Discussions

In this paper, we are using the value of parameters \( R \) and \( C \) using 90 nm technologies. So the exact values of the parameter \( R \) and \( C \) using 90 nm technologies [1] are given in Table 1.

<table>
<thead>
<tr>
<th>Parameter(s)</th>
<th>Value/mm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resistance(R)</td>
<td>13Ω/mm</td>
</tr>
<tr>
<td>Capacitance(C)</td>
<td>0.45pF/mm</td>
</tr>
</tbody>
</table>

Expressions given by equations (21) and (29) represent the theoretical and closed form formulae for maximum noise amplitude and width of noise voltage for proposed 2-π model. These expressions are verified and tested on randomly generated multi-pin nets with general RC tree structures and the efficiency of the proposed models are justified when compared to SPICE simulations. To obtain high fidelity and to detect the corner scenarios, we run our 2π model on 1000 randomly generated circuits with realistic parameters in a 90 nm technology. For the test circuits, the driver resistance \( R_d \) is from 100 to 500 Ω, the loading capacitance \( C_L \) is from 10 to 100fF, the length parameters \( L_s, L_c, \) and \( L_e \) are from 1 to 2500 μm, the wire width/spacing is either 1x or 2x minimum width/spacing, and the aggressor slew is from 50 to 500 ps.

Table 2 discusses the comparative study in between proposed model crosstalk noise voltage with SPICE crosstalk values for different aggressor slews for randomly selected parameter values. From Table 2, it can be analyzed that error presented by this model is less than 1% on average compared with SPICE simulation, for peak noise crosstalk voltage.
Table 2: Comparison of Proposed Crosstalk Noise Voltage with SPICE result values for different Aggressor Slew in a 90 nm Technology

<table>
<thead>
<tr>
<th>R_D1 (Ω)</th>
<th>R_D2 (Ω)</th>
<th>C_L (F)</th>
<th>T_s=100</th>
<th>T_s=200</th>
<th>T_s=500</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>SPICE Values (mV)</td>
<td>Proposed Model Values (mV)</td>
<td>SPICE Values (mV)</td>
</tr>
<tr>
<td>100</td>
<td>100</td>
<td>10</td>
<td>83</td>
<td>91</td>
<td>128</td>
</tr>
<tr>
<td>200</td>
<td>250</td>
<td>50</td>
<td>123</td>
<td>131</td>
<td>167</td>
</tr>
<tr>
<td>300</td>
<td>350</td>
<td>70</td>
<td>143</td>
<td>148</td>
<td>182</td>
</tr>
<tr>
<td>400</td>
<td>500</td>
<td>100</td>
<td>157</td>
<td>156</td>
<td>203</td>
</tr>
</tbody>
</table>

Table 3: Comparison of Proposed Noise Width with SPICE result values for different Aggressor Slew in a 90 nm Technology

<table>
<thead>
<tr>
<th>R_D1 (Ω)</th>
<th>R_D2 (Ω)</th>
<th>C_L (F)</th>
<th>T_s=100</th>
<th>T_s=200</th>
<th>T_s=500</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>SPICE Values (ns)</td>
<td>Proposed Model Values (ns)</td>
<td>SPICE Values (ns)</td>
</tr>
<tr>
<td>100</td>
<td>100</td>
<td>10</td>
<td>4.54</td>
<td>3.89</td>
<td>7.23</td>
</tr>
<tr>
<td>200</td>
<td>250</td>
<td>50</td>
<td>7.59</td>
<td>7.43</td>
<td>10.65</td>
</tr>
<tr>
<td>300</td>
<td>350</td>
<td>70</td>
<td>8.52</td>
<td>9.01</td>
<td>12.38</td>
</tr>
<tr>
<td>400</td>
<td>500</td>
<td>100</td>
<td>12.34</td>
<td>11.96</td>
<td>15.28</td>
</tr>
</tbody>
</table>

Table 3 discusses the comparative study in between proposed model noise width with SPICE values for different aggressor slews for randomly selected parameter values.

V. CONCLUSION

In this paper presents a reduction and optimizations of crosstalk and driver sizing in much improved 2-π model using 90nm process technology parameters. In this paper we consider a step input signal for the excitation of aggressor line. Different sensitivity expressions are derived for the driver sizing and spacing. By considering the signs of sensitivity expressions, effect of driver sizing spacing (aggressor net and victim net) on crosstalk noise amplitude and width can be examined.
REFERENCES