

DESIGN AND SIMULATION OF 2-TO-4 DECODER USING SINGLE ELECTRON TUNNELING TECHNOLOGY BASED THRESHOLD LOGIC GATE

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Received 26 January 2011, Accepted 1 February 2011, Revised 15 April 2011

ABSTRACT

Single electron devices have ultra-low power consumption and high integration density which makes them promising candidates as basic circuit elements of the next generation ultra-dense VLSI and ULSI circuits. In this paper, design, simulation and analysis of 2-to-4 decoder using single-electron tunnelling technology based threshold logic gate is presented. The circuit consists of four buffered threshold logic gates. The logic operation of the circuit is simulated and verified using Monte Carlo simulation. The free energy history and stability diagram verified the correct functioning of the circuit.

Keywords: Coulomb blockade, Single electron tunnelling technology, Tunnel Junction, Critical voltage, Threshold logic gate, 2-to-4 decoder.

1. INTRODUCTION

The CMOS technology will presumably be continued up to the year 2014 by the well-known scaling of structure geometry [1]. However, there have been reports suggesting that the CMOS transistor can not shrunk beyond certain limits dictated by its operating principle [2]. Over recent years this realization has led to exploration of possible successor technologies with greater scaling potential such as quantum and single electronics for the next generation VLSI/ULSI circuits. The Single Electron Tunnelling (SET) technology is one of the most promising future technologies to meet the required increase in density, performance and decrease in power dissipation [3-8]. While the prospect of CMOS devices being completely replaced by SET devices remains to be seen, SET devices and circuits have received tremendous attention in the research community.

Most of the single-electron circuits have been implemented by representing Boolean functions as a network of single-electron AND, OR and NOT logic gates. The performance of Boolean function based implementation might be severely affected by a large circuit depth and alternative solutions are required. A potential alternative to Boolean Logic is the Threshold Logic [6]. A number of investigations have been reported regarding the possibilities of threshold logic based design and implementations of useful Boolean functions [9-14]. The design and simulation of single electron 2-to-4 decoder have been reported in literature [15, 16, 17]. Since single electron tunneling technology based threshold logic design is an emerging area for development of future low power ultra-dense VLSI/ULSI circuits, it is important to design, simulate and analyze single electron circuits using threshold logic gates. All these have motivated us to design, simulate and analyze 2-to-4 decoder using single electron technology based threshold logic gate.

In this work, design, simulation and analysis of 2-to-4 decoder using SET based threshold logic gate is presented. The logic operation of the decoder is simulated using SIMON2 which is a single-electron circuit simulator based on Monte Carlo method to verify the correct functioning of the circuit. To confirm the stable operation of the circuit, free energy history and stability plot have been constructed using SIMON2.

2. THE BASIC PHYSICS

The basic component of single electron tunnelling technology is the tunnel junction. A tunnel junction can be considered as two conductors separated by a thin layer of insulating material. A tunnel junction and its schematic diagram are shown in Figure 1. It is characterised by a capacitance C_j and a

resistance R_j , each of which depends on the physical size of the tunnel junction and the thickness of the insulator. The fundamental principle of SET devices and circuits is the Coulomb blockade, which was first observed and studied by Gorter [18].

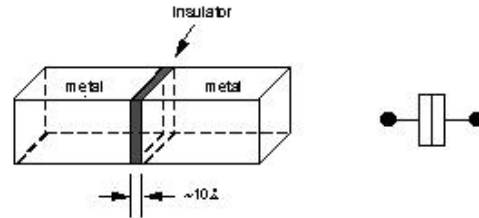


Fig. 1. Schematic Structure and Symbol of Tunnel Junction

The transport of electron through a tunnel junction is called tunnelling. Electrons are considered to tunnel through a tunnel junction one after another [7, 8, 19]. Even only one electron tunnelling may produce a voltage e/C across the tunnel junction (where C is total capacitance and $e =$ electronics charge $= 1.602 \times 10^{-19}$ C). According to orthodox theory [20, 21] the critical voltage V_c , which is the minimum voltage across the tunnel junction to make an electron tunnel possible can be calculated as

$$V_c = \frac{e}{2(C_e + C_j)} \quad (1)$$

Where $e=1.602 \times 10^{-19}$ C, C_j is the tunnel junction capacitance and C_e is the equivalent capacitance for remainder circuit as viewed from the tunnel junction's perspective. Tunnel event will occur across the tunnel junction if and only if the voltage V_j across the tunnel junction is greater than or equal to V_c i.e $|V_j| \geq V_c$, otherwise the tunnel event cannot occur. This phenomenon is also called Coulomb blockade. The circuit will be in stable state if $|V_j| < V_c$. Due to the stochastic nature of electron tunnelling, the switching delay is described as [8]

$$t_d = \frac{-\ln(P_{error})eR_j}{|V_j| - V_c} \quad (2)$$

where P_{error} is the probability that the tunnel event has not occurred after t_d seconds. The energy consumed by a switching activity can be calculated by determining the difference in the total amount of energy present in a circuit before and after a tunnel event which can be calculated by [8]

$$\Delta E = E_{initial} - E_{final} = e(|V_j| - V_c) \quad (3)$$

Tunnel event will occur across the tunnel junction if and only if the voltage V_j across the tunnel junction is greater than or equal to V_c i.e $|V_j| \geq V_c$, otherwise the tunnel event cannot occur. The circuit will be in stable state if $|V_j| < V_c$.

3. THRESHOLD LOGIC GATE

A threshold logic gate is a device which is able to compute any linearly separable Boolean function given:

$$Y = \text{sgn}\{F(X)\} = \begin{cases} 0 & \text{if } F(X) < 0 \\ 1 & \text{if } F(X) \geq 0 \end{cases} \quad (4)$$

where $F(X) = \sum_{i=1}^n w_i x_i - T$, x_i are the n Boolean inputs and w_i are the corresponding n integer weights. The gate symbol of a threshold logic gate (TLG) is shown in Figure 2. The TLG performs a comparison between the weighted sum of inputs $\sum_{i=1}^n w_i x_i$ and the threshold value T . If the weighted sum of inputs is greater than or equal to the threshold, the gate produces logic 1 at the output; otherwise output is logic 0. A generic SET-based threshold logic gate proposed by C. Lageweg et al [8] is shown in Figure 3.

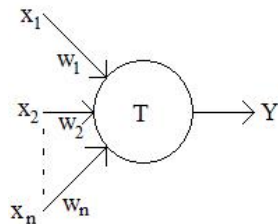


Fig. 2. TLG Gate symbol

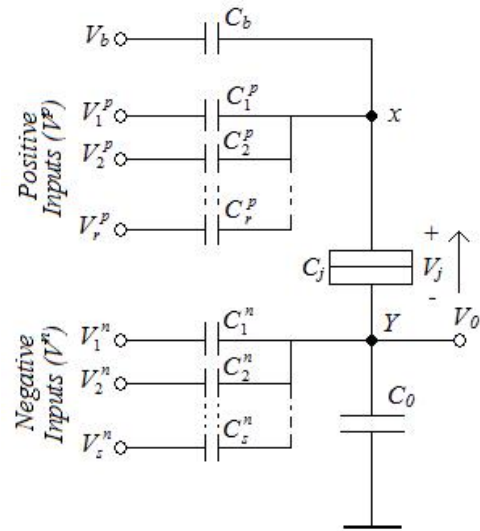


Fig. 3. TLG structure

The input voltages V^p weighted by their input capacitances C^p are added to V_j and the input voltages V^n weighted by their input capacitances C^n are subtracted from V_j . The critical voltage V_c of the tunnel junction which can be adjusted by the bias voltage V_b weighted by C_b acts as the threshold value. The function $F(X)'$ for the circuit is given by [8, 22]

$$F(X)' = C_{\Sigma}^n \sum_{k=1}^r C_k^p V_k^p - C_{\Sigma}^p \sum_{l=1}^s C_l^n V_l^n - T' \quad (5)$$

where

$$T' = \frac{1}{2} (C_{\Sigma}^p + C_{\Sigma}^n) - C_{\Sigma}^n C_b V_b, \quad (6)$$

$$C_{\Sigma}^p = C_b + \sum_{k=1}^r C_k^p \quad (7)$$

$$C_{\Sigma}^n = C_0 + \sum_{l=1}^n C_l^n \quad (8)$$

Detailed derivation of the above equations can be found in Ref. [23]. This gate is able to implement certain Boolean function if the involved parameters are chosen properly.

4. DESIGN OF 2-TO-4 DECODER

The truth table of a 2-to-4 decoder is given in Table I and the Boolean gate based implementation is shown in Figure 4. The

Boolean gate-based implementation of 2-to-4 decoder required six gates and a logic network with a depth of two.

Table I: Truth Table of 2-to-4 decoder

Inputs		Outputs			
X	Y	D0	D1	D2	D3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

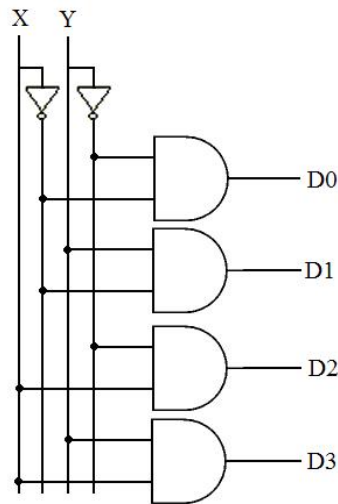


Fig. 4. Boolean gate based implementation of 2-to-4 decoder

The 2-to-4 decoder can be realized using only four threshold logic gates and a network depth of one. The threshold logic equations for the outputs of the decoder can be written as

$$D0 = \text{sgn}\{-X - Y + 0.5\} \quad (9)$$

$$D1 = \text{sgn}\{-X + Y - 0.5\} \quad (10)$$

$$D2 = \text{sgn}\{X - Y - 0.5\} \quad (11)$$

$$D3 = \text{sgn}\{X + Y - 1.5\} \quad (12)$$

It was proposed that [8, 22] a SET buffer/inverter depicted in Figure 5 should follow the threshold logic structure to provide enough driving ability and stability.

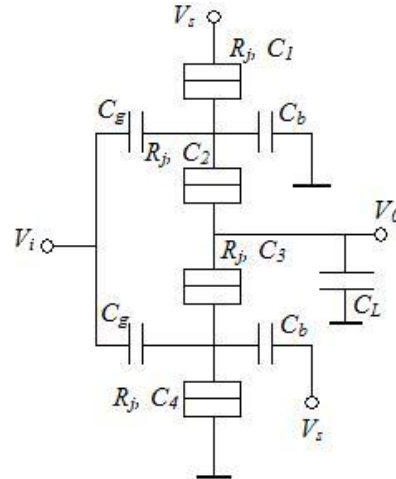


Fig 5. SET Buffer/Inverter

Since the buffer/inverter inverts the output of the original threshold logic, we need to reverse the positively and negatively weighted inputs in the logic function accordingly. The threshold logic equations for the outputs in the case of buffered threshold logic gates can be written as

$$D0 = \text{sgn}\{X + Y - 0.5\} \quad (13)$$

$$D1 = \text{sgn}\{X - Y + 0.5\} \quad (14)$$

$$D2 = \text{sgn}\{-X + Y + 0.5\} \quad (15)$$

$$D3 = \text{sgn}\{-X - Y + 1.5\} \quad (16)$$

The resulting 2-to-4 decoder implementation which consists of four buffered threshold logic gates (TLG0-TLG3) is shown in Figure 6.

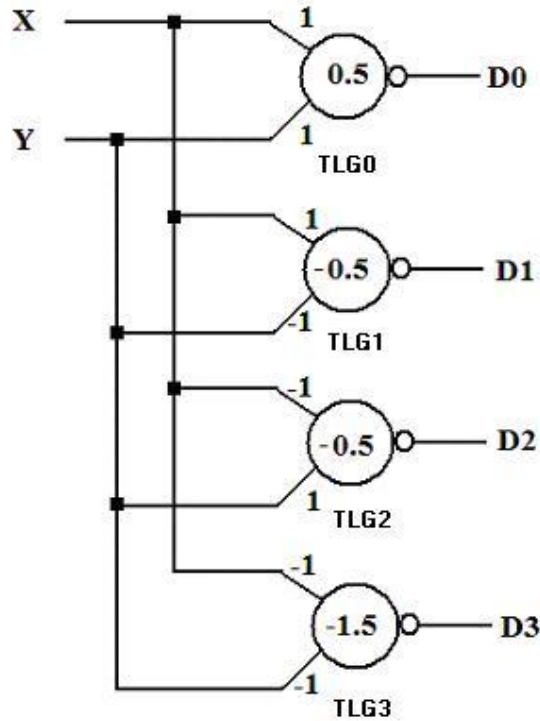


Fig. 6. 2-to-4 decoder implementation in threshold gate

5. DESIGN OF THRESHOLD GATES (TLG0-TLG3)

When combining a threshold logic gate with buffer/inverter the buffer adds an additional capacitive load to the logic gate's output node. The buffer's supply voltage and output voltage change the logic gate's biasing due to a feedback effect. This effect is accounted for by considering an additional negatively weighted input V_{buff}^n capacitively coupled to the threshold gate with an input capacitance C_{buff}^n and the threshold value of each threshold gates must be adjusted by $-V_{buff}^n C_{buff}^n C_{\Sigma}^p$. To determine the parameter values of TLG0 - TLG3, we assume the following voltage levels: Logic 0=0 V, Logic 1= $0.1e/C=16$ mV, $R_j=100K\Omega$ and $C_j=0.1C$, where $C=1aF$ is used as a unit of capacitance. For the buffer/inverter, circuit parameters values are taken from Ref. 8. Comparing equations (5) and (13), we

obtained the following relation for the weights of TLG0.

$$C_{\Sigma}^n C_1^p = C_{\Sigma}^n C_2^p \tag{17}$$

Given the choice of logic level 1, we want the change in output voltage due to transport of an electron to be equal to $0.1e/C$. The change in output voltage due to transport of an electron in the arrow's direction in the generic SET-based threshold gate is given by [23]

$$dV_0 = eC_{\Sigma}^p / C_{\tau} \tag{18}$$

where

$$C_{\tau} = C_{\Sigma}^p C_{\Sigma}^n + C_{\Sigma}^p C_j + C_{\Sigma}^n C_j \tag{19}$$

We assume $C_j \ll C_{\Sigma}^p$ and $C_j \ll C_{\Sigma}^n$ to ensure that a large percentage of the input voltages are applied over the tunnel junction due to capacitive division and equation (19) reduces to

$$C_{\tau} = C_{\Sigma}^p C_{\Sigma}^n \tag{20}$$

$$dV_0 = eC_{\Sigma}^p / C_{\tau} = e / C_{\Sigma}^n = 0.1e/C$$

$$\Rightarrow C_{\Sigma}^n = 10C$$

For a buffered TLG, $C_{\Sigma}^n = C_0 + 1C$, therefore $C_0 = 9C$. We also assume input capacitors which are small compared to C_{Σ}^n in order to limit the capacitive division effect of the inputs on the output. By choosing $C_0 = 9C$ and $V_b = 16mV$, we now have C_b to be the only parameter to be determined with its value depending on the specific threshold logic expression. From the threshold equation of TLG0 (equation (13)) it is clear that when X is at logic 1, it contributes 1 to the weighted sum of the gate inputs. The same is true for input X. If we now apply logic 1 (i.e $0.1e/C$ V) to X and Y inputs of the TLG0, equation (5) becomes

$$\begin{aligned} F(X)^/ &= \\ C_{\Sigma}^n \sum_{k=1}^r C_K^p V_K^p - C_{\Sigma}^p \sum_{l=1}^S C_l^n V_l^n - T^/ & \\ = C_{\Sigma}^n C_1^p V_1^p + C_{\Sigma}^n C_2^p V_2^p - T^/ & \end{aligned}$$

$$= 10C[0.5C \times 0.1e/C + 0.5C \times 0.1e/C - T']$$

$$= 0.5eC + 0.5eC - T' = \alpha + \alpha - T'$$

Applying logic 1 to any input of TLG0 translate into a contribution of $\alpha=0.5eC$. Therefore α act as a scaling factor and T should also be scaled by α i.e $T' = \alpha T = 0.5 \times 0.5eC = 0.25eC$. With adjustment for buffered threshold gate, the new threshold value is given by $0.25eC - 0.046eC \sum$ and substituting this value in eqn. (6), we get

$$0.25eC - 0.046eC \sum^p = \dots\dots \tag{21}$$

$$e(C_{\sum}^n + C_{\sum}^p) / 2 + C_{\sum}^n C_b V_b$$

From eqn. (21), the value of C_b is obtained as $11.7C$. Following the same procedure, the following parameters are obtained for other threshold gates.

TLG1: $C_1^n = C_1^p = 0.5C, V_b = 18.037mV,$

$C_b = 9.5C, C_0 = 8.5C$

TLG2: $C_1^n = C_1^p = 0.5C, V_b = 18.037mV,$

$C_b = 9.5C, C_0 = 8.5C$

TLG3: $C_1^n = C_2^n = 0.5C, V_b = 16mV$

$, C_b = 13.2C, C_0 = 8C$

6. SIMULATION RESULTS AND ANALYSIS

The logic operations of TLG0-TLG3 are first examined independently by simulation using Monte Carlo simulation software SIMON2 [21, 24]. The simulated circuit and input-output waveforms of TLG0 are depicted in figures 7 and 8. The logic operation is found to be correct. For TLG1-TLG3, the simulated circuits and their input and output waveforms are given in figures 9-14. The results obtained from the simulation are found to be satisfactory. All the four threshold gates (TG0 - TG3) are

connected to implement the 2-to-4 decoder. The circuit simulated using SIMON2 is shown in Figure 15. All the possible combination of the inputs (X and Y) and the outputs (D0-D3) of the circuit is depicted in Figure 16. The logic operation of the circuit is found to be satisfactory.

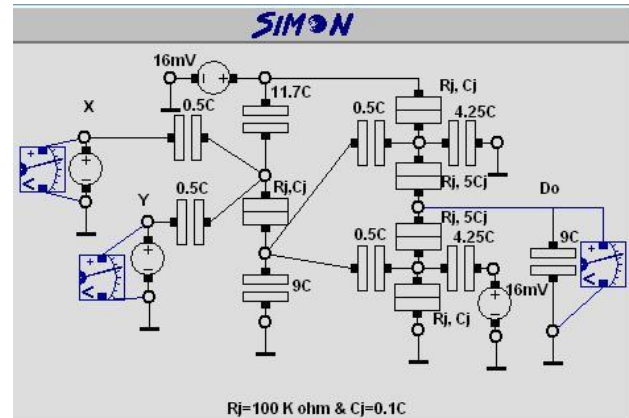


Fig 7. Circuit for TLG0

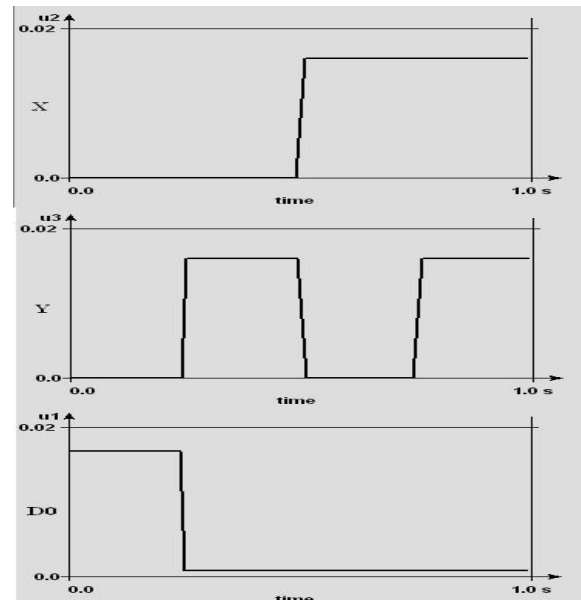


Fig 8. Input-output waveforms of TLG0

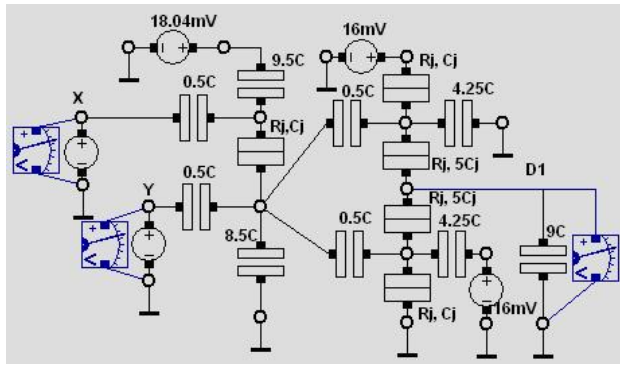


Fig. 9. Circuit for TLG1

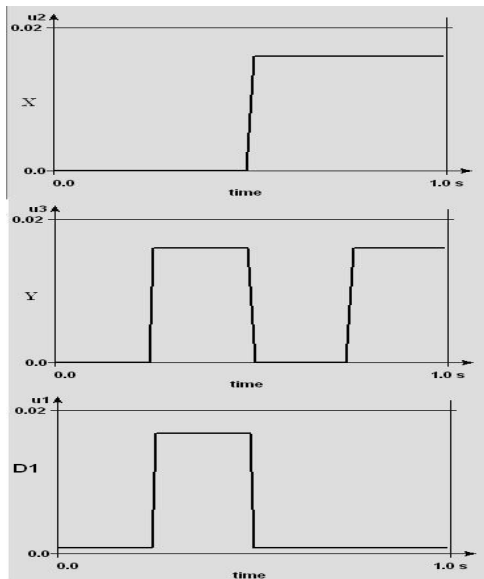


Fig.10. Input-output waveforms of TLG1

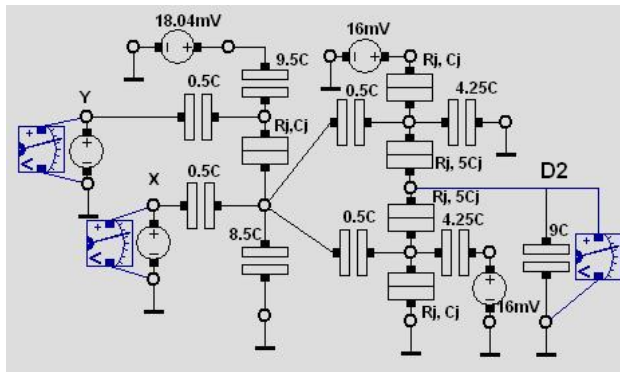


Fig. 11. Circuit for TLG2

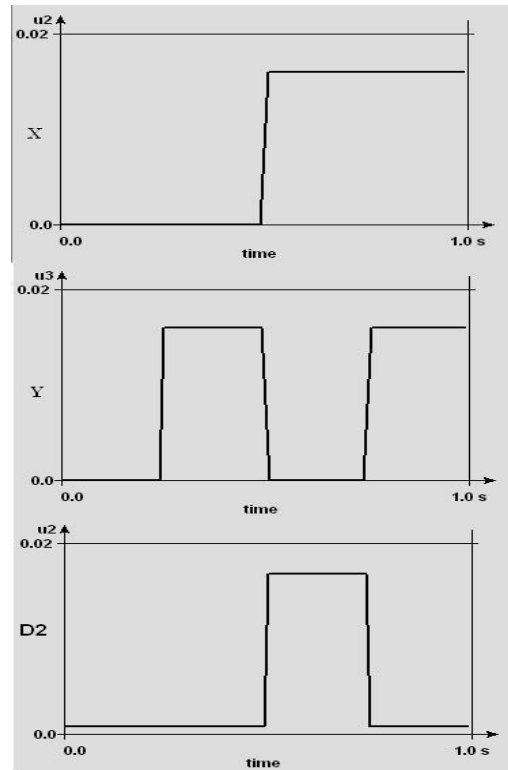


Fig. 12. Input-output waveforms of TLG2

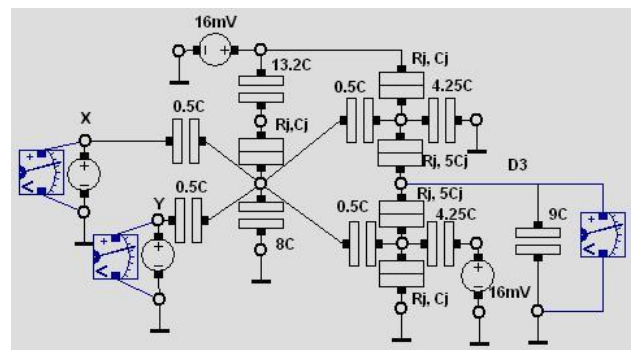


Fig. 13. Circuit for TLG3

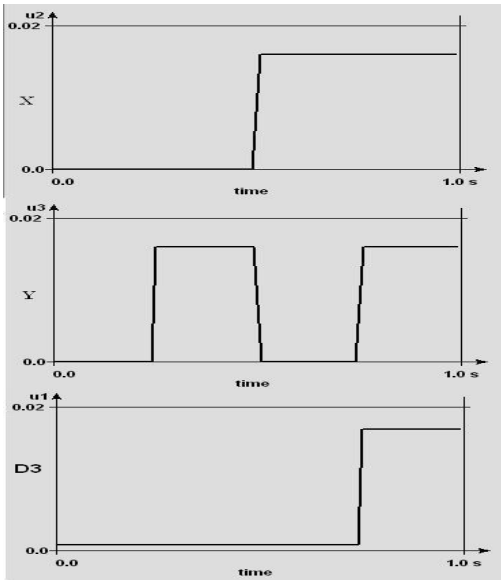


Fig. 14. Input-output waveforms of TLG3

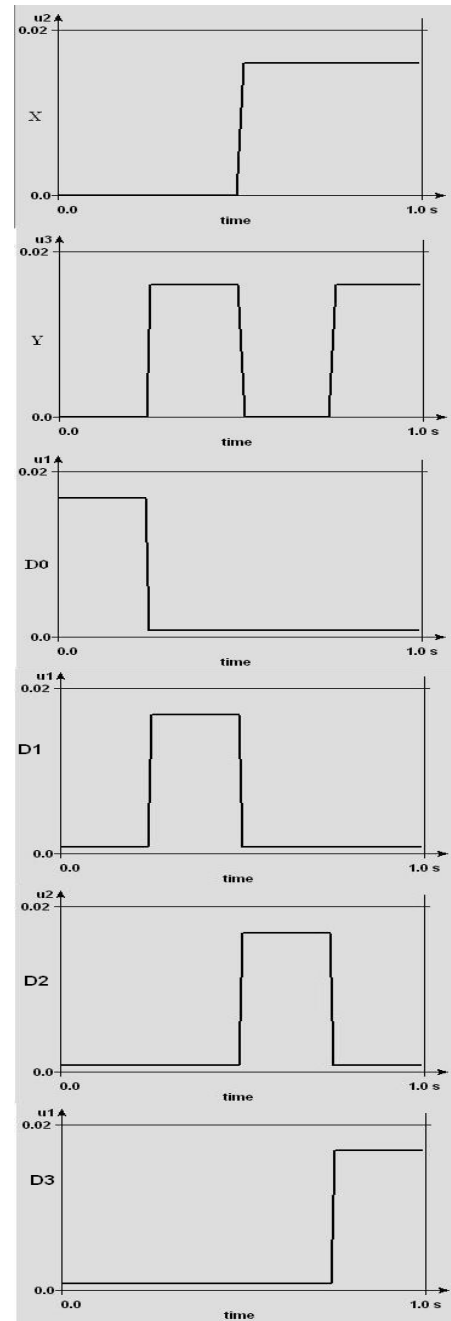


Fig.16. Input-Output waveforms of 2-to-4 decoder

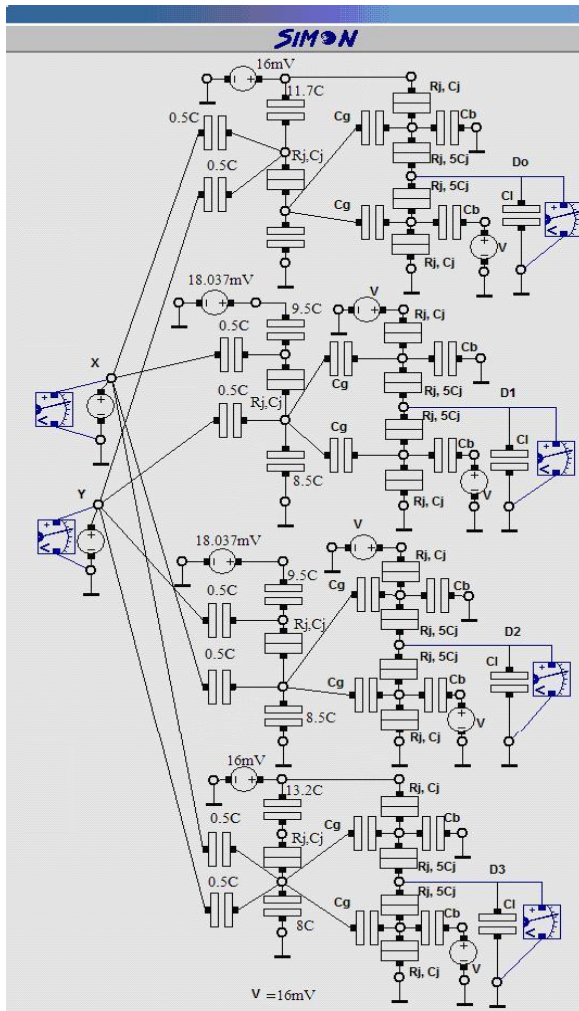


Fig. 15. 2-to-4 decoder circuit simulated using SIMON2

The stability of the 2-to-4 decoder is studied by constructing its free energy history diagrams and stability plots. The free energy history of the circuit is tested at four output points, D0–D3, during a transition of the output from 0 to 1. The output transition from 0 to 1 is achieved by transporting an

electron from the output node to supply voltage through two tunnel junctions. All the output points are found to have a similar free energy history diagram which is shown in figure 17. Both logic 0 and logic 1 states of four output points correspond to energy minima. This is a strong indication of gate stability. To confirm the stable operation of the circuit, its stability plots have been constructed using SIMON2. Figure 18 shows the two dimensional sections of the stability plot. The four possible combinations of the inputs (X & Y) are represented by points 1, 2, 3 and 4. It is clear that all points are located into stable regions, i.e. in white and gray, which are stable enough to allow the desired operation of the circuit shown in figure 15.

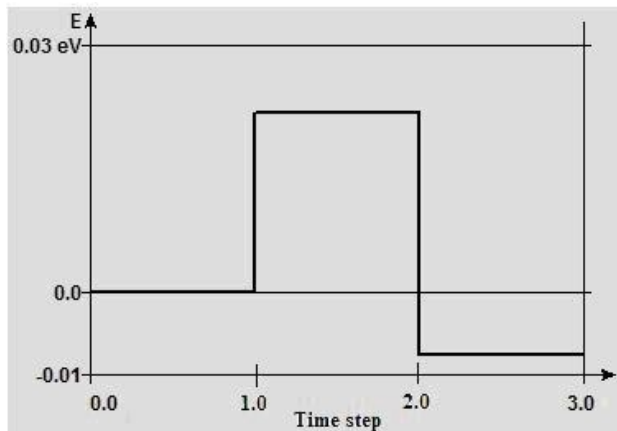


Fig. 17. Free energy history

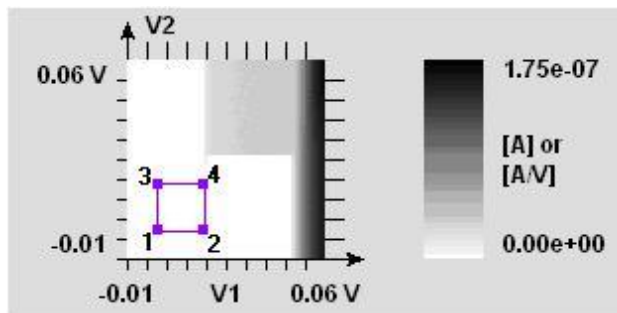


Fig. 18. Stability plot of the circuit. 1: X=0, Y=0, 2: X=0, Y=1, 3: X=1, Y=0 and 4: X=1, Y=1

7. CONCLUSION

The design, simulation and analysis of 2-to-4 decoder using single electron tunnelling technology based threshold logic gate is presented. The performance of the proposed circuit is verified by simulation using SIMON2. The free energy history diagrams and stability plot shows that the circuit presented in this paper is stable thereby establishing the feasibility of using the proposed circuit in future low power ultra-dense VLSI/ULSI circuits.

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