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An Analytical Subthreshold Drain Current Model for Pocket Implanted Nano Scale n-MOSFET

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Abstract: *This paper presents an analytical subthreshold drain current model for pocket implanted nano scale n-MOSFET. The model is developed by using the linear pocket profiles at the source and drain edges and by solving the Poisson's equation in the depletion region at the surface with the appropriate boundary conditions at source and drain for deriving the surface potential. The model includes the effective doping concentration of the two linear pocket profiles. Electron current density is obtained from the conventional drift-diffusion equation. Integration of surface potential is obtained numerically. Effective channel thickness is obtained by applying Gauss's Law at the surface. The simulation results show that the derived subthreshold drain current model has a simple compact form that can be utilized to study and characterize the pocket implanted advanced ULSI MOS devices.*

Keywords: *Linear Pocket Profile, Pocket Implanted MOSFET, Subthreshold Drain Current, Surface Potential, Threshold Voltage*

1. INTRODUCTION

As the channel length of MOSFETs is scaled down to deep-submicrometer or sub-100 nm regime, we observe the reduction of threshold voltage with the reduction of channel length due to the charge sharing between the drain/source region and the channel [1]. Also, the off-state leakage current increases due to sensitivity of the source/channel barrier to the drain potential or drain induced barrier lowering (DIBL). This effect is known as short-channel effect (SCE). This effect arises as a result of two dimensional potential distribution and high electric fields in the channel region [2]. It can be reduced or can be even reversed (then it is called reverse short channel effect or RSCE in short) by locally raising the channel doping near source and drain junctions. RSCE was originally observed in MOSFETs due to oxidation-enhanced-diffusion [3] or implant-damage-enhanced diffusion [4] which are very difficult to control. Lateral channel engineering utilizing halo or pocket implant [5-9] surrounding drain and source regions is effective in suppressing short channel effects. The halo or pocket implant can be either symmetrical [10] or asymmetrical [11] with respect to source or drain. Reported circuit applications include a 256 M-bit DRAM [12] and mixed-signal processor [13]. In fact, this pocket implant technology is found to be very promising in the effort to tailor the short-channel performances of deep-submicron as well as sub-100 nm MOSFETs although careful tradeoffs need to be made between minimum channel length and other device electrical parameters [6].

Already few papers have been published focusing on the subthreshold behaviour of pocket implanted MOSFET [14-16]. When the gate voltage is below the threshold voltage and the semiconductor surface is in weak inversion, the corresponding drain current is called the subthreshold current. The subthreshold region is particularly important for low-voltage, low-power applications, such as when the MOSFET is used as a switch in digital logic and memory applications, because the subthreshold region describes how the switch turns on and off. In [9], models for subthreshold and above subthreshold currents in 0.1 μm pocket n-MOSFETs for low-voltage applications have been derived based on the diffusion current transport equation. But this model characterizes the localized pile-up of channel dopants as step profile. The influences of halo implant dose and tilt angle on the off-state current have been investigated by technology computer-aided design (TCAD) simulation in [14]. A channel length independent subthreshold characteristic in submicron MOSFETs has been reported by Shin et al in [15] due to the presence of localized pileup of channel dopants near the source and drain ends of the channel. An analytical subthreshold current model for pocket-implanted n-MOSFETs has been presented in [16]. But this model also characterizes the localized channel dopants as step profile.

In this paper, an analytical subthreshold current model for the sub-100 nm pocket implanted n-MOSFET has been derived assuming the linear profiles of pocket doping. Here the 1-D pocket profiles across the channel have been transformed to an effective doping concentration expression, which is used in the 1-D Poisson’s equation to derive the surface potential model applying the

appropriate boundary conditions at the source and drain. The effective channel thickness is found applying Gauss's law. Finally, the current equation is obtained from the conventional drift-diffusion equation. Simulation results show that the model predicts subthreshold current very well for various device and pocket profile parameters as well as various bias conditions. It proves the validity and usefulness of our proposed model for circuit simulation of next generation ULSI devices.

2. POCKET DOPING PROFILE

The pocket implanted n-MOSFET structure shown in Fig. 1 is considered in this work and assumed co-ordinate system is shown at the right side of the structure. All the device dimensions are measured from the oxide-silicon interface. In the structure, the junction depth (r_j) is 25 nm. The oxide thickness (t_{ox}) is 2.5 nm, and it is SiO_2 with fixed oxide charge density of 10^{11} cm^{-2}. Uniformly doped p-type Si substrate is used with doping concentration of $N_{sub} = 4.2\times10^{17}$ cm^{-3} with pocket implantation both at the source and drain side with peak pocket doping concentration of $N_{pm} = 1.75\times10^{18}$ cm^{-3} and pocket length of $L_p = 25$ nm, and the source or drain doping concentration of $N_{sd} = 9.0\times10^{20}$ cm^{-3}.

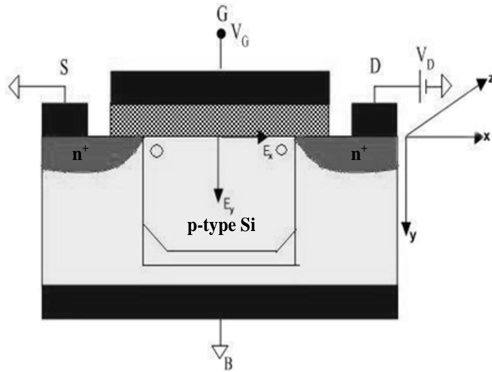

Fig. 1 Pocket implanted n-MOSFET structure.

The pocket implantation, which causes the Reverse Short Channel Effect (RSCE), is done by adding impurity atoms both from the source and drain edges. It is assumed that the peak pocket doping concentration, N_{pm} gradually decreases linearly towards the substrate level concentration, N_{sub} with a pocket length, L_p from both the source and drain edges. The basis of the model of the pocket profile is to assume two linear doping profiles from both the source and drain edges across the channel as shown in Fig. 2. The pocket parameters, N_{pm} and L_p, play important role in determining the RSCE.
At the source side, the pocket profile is given as:

$$N_s(x) = N_{sub}\frac{x}{L_p} + N_{pm}\left(1 - \frac{1}{L_p}x\right) \tag{1}$$

At the drain side, the pocket profile is given as:

$$N_d(x) = N_{sub}\left(\frac{L}{L_p} - \frac{1}{L_p}x\right) + N_{pm}\left(1 - \frac{L}{L_p} + \frac{1}{L_p}x\right) \tag{2}$$

,where x represents the distance across the channel from source to drain. Since the pile-up profile is due to the direct pocket implant at the source and drain side, it is assumed symmetric at both sides.

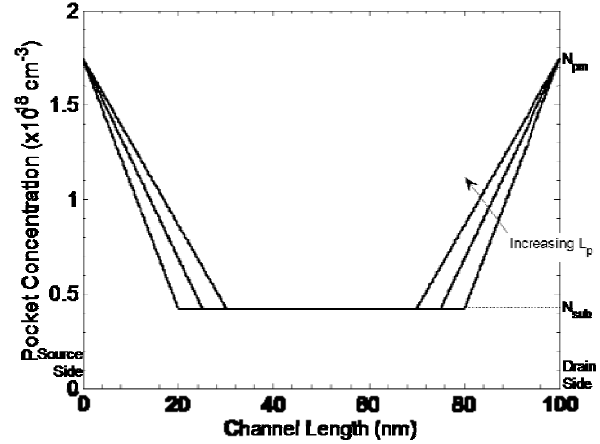

Fig. 2 Simulated pocket profiles at the surface for different pocket lengths, L_p = 20, 25 and 30 nm. Peak pocket concentration, $N_{pm} = 1.75\times10^{18}$ cm^{-3}.

The conceptual pocket profiles given in equations (1) and (2) are then integrated mathematically along the channel and then divided by the channel length to derive an average effective channel doping concentration as in equation (3).

$$N_{eff} = N_{sub}\left(1 - \frac{L_p}{L}\right) + \frac{N_{pm}L_p}{L} \tag{3}$$

When $L_p << L$ for long channel device then pocket profile has no effect on the subthreshold current, but when L_p is comparable with L for short channel device then the pocket profile affects the subthreshold current.

3. SUBTHRESHOLD CURRENT MODEL

Based on the drift-diffusion equation, the electron current density J_n in an n-MOSFET can be written as

$$J_n = q\left(-n\mu_n\frac{d\psi_s}{dx} + D_n\frac{dn}{dx}\right) = qD_n\left(\frac{-n}{V_{th}}\frac{d\psi_s}{dx} + \frac{dn}{dx}\right) \tag{4}$$

,where $\psi_s(x)$, n, D_n and q is are the surface potential, electron density, diffusion co-efficient and electronic charge. V_{th} is the thermal and is given as follows

$$V_{th} = \frac{kT}{q} = \frac{D_n}{\mu_n} \tag{5}$$

We assume the following boundary conditions:

1. At $x = 0$, i.e. at the source side, the surface potential is $\psi_s(0) = \varphi_{bi} - V_{BS}$.

2. At $x = L$, i.e. at the drain end, the surface potential is $\psi_s(L) = \varphi_{bi} - V_{BS} + V_{DS}$, where V_{BS}, V_{DS} and φ_{bi} are the substrate bias, drain bias and source/drain junction built-in potential respectively.

Multiplying equation (1) by an integrating factor of $e^{-\psi_s/V_{th}}$, the right hand side of equation (4) can be transformed into an exact derivative and using the above boundary conditions, we get the following equation

$$J_n = -qD_n N_{eff} \exp\left(-\frac{\varphi_{bi} - V_{BS}}{V_{th}}\right) \frac{\left(1 - \exp\left(\frac{V_{DS}}{V_{th}}\right)\right)}{\int_0^L \exp\left(-\frac{\psi_s}{V_{th}}\right) dx} \qquad (6)$$

After solving the 2nd order Poisson's equation using the above two boundary conditions, the complete analytical surface potential expression (ψ_s) was found in [17], and will be used in equation (6) to calculate the current density (J_n).

The integral in the denominator of the right hand side of equation (6) is evaluated using the numerical integration technique of multiple segments Simpson's 1/3 rule and the surface potential model given in equation (7).

Finally, the drain current, I_{ds} in the channel is obtained by multiplying J_n and the channel cross-sectional area (which is the multiplication of effective channel thickness, t_{ch} and channel width, W) as given in equation (8).

$$I_{ds} = J_n W t_{ch} \qquad (8)$$

The effective channel thickness, t_{ch} can be obtained as the distance from the surface to the position along the y-direction where the electrostatic potential has changed by V_{th} [18]. When the gate voltage V_{GS} is in the close vicinity of the threshold voltage, the drain current I_{ds} becomes the subthreshold current, I_{sub}. By using Gauss' law, the vertical component of the electric field at the surface, V_{th}/t_{ch}, is equal to Q_{dep}/ε_s in the subthreshold region. Thus the effective channel thickness is found as in equation (9).

$$t_{ch} = V_T \sqrt{\frac{\varepsilon_s}{2qN_{eff}\left(2\varphi_F - V_{BS} + V_{GT}/\theta\right)}} \qquad (9)$$

,where $V_{GT} = V_{GS} - V_T$, θ is the subthreshold ideality factor reflecting the gate voltage division between the insulator capacitance and the depletion layer capacitance and φ_F is the Fermi potential due to pocket implantation and is given as in equation (10).

$$\varphi_F = \frac{kT}{q} \ln \frac{N_{eff}}{n_i} \qquad (10)$$

Threshold voltage, V_T for this calculation is taken from [19]. The effective channel thickness given in equation (9) is only valid when $-\psi(s) + V_{BS} < V_{GT}/\theta$, i.e., in the weak inversion and depletion regions.

4. RESULTS AND DISCUSSIONS

In order to verify the analytical subthreshold current model for the pocket implanted n-MOSFET, different types of simulations were performed.

From Fig. 3 it is observed that as the drain bias increases, both RSCE and SCE occur at longer channel length due to the drain induced barrier lowering (DIBL). As channel length becomes shorter DIBL effect is more pronounced. Higher drain bias makes the threshold voltage negative. Since at shorter channel length, electric field is very high and it lowers the potential barrier that separates it from the adjacent diffused junction.

In Figs. 4 (a)-(b) subthreshold current variation for different gate voltages are shown for two different drain biases with channel lengths of 0.25 μm and 100 nm. It is observed that for longer channel length device, subthreshold current does not change appreciably as the drain bias increases, but for shorter channel length device, subthreshold current changes appreciably as the drain bias increases. This also occurs due to significant DIBL effect.

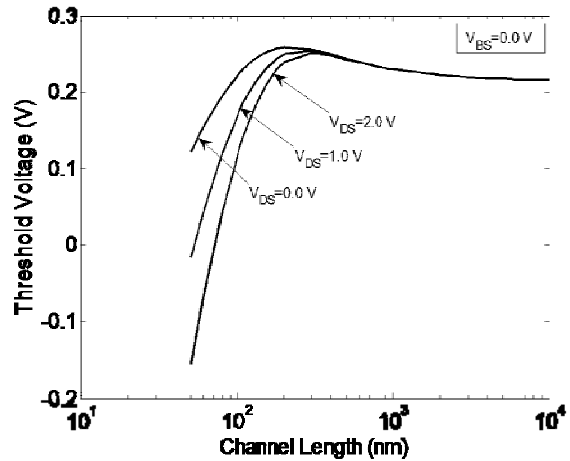

Fig. 3 Threshold voltage vs. gate length curves for various drain biases at zero substrate bias.

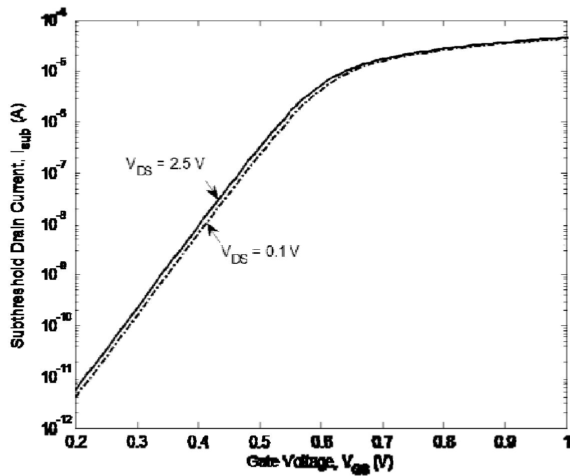

Fig. 4 (a) Subthreshold drain current versus gate voltage for two drain biases of V_{DS} = 0.1 V and V_{DS} = 2.5 V with channel length, L = 0.25 μm.

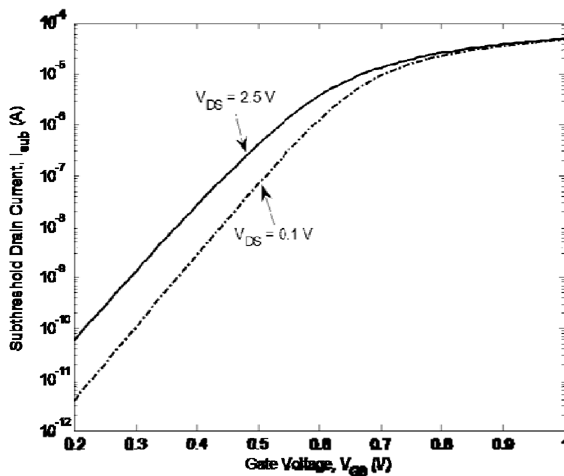

Fig. 4 (b) Subthreshold drain current versus gate voltage for two drain biases of V_{DS} = 0.1 V and V_{DS} = 2.5 V with channel length, L = 100 nm.

Fig. 5 shows the variation of subthreshold drain current variation with gate voltage for three different peak pocket concentration. It is observed that as the peak of the pocket implant concentration decreases the subthreshold current increases for the same applied gate bias. This happens due to the additional doping atoms present near the source and drain edges. It is also observed that as the peak pocket implant concentration decreases more then the subthreshold slope decreases. Because then RSCE diminishes.

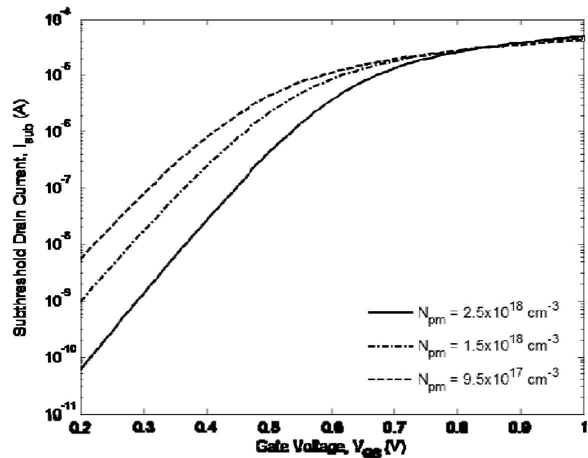

Fig. 5 Subthreshold drain current versus gate voltage for three peak pocket concentration, drain bias, V_{DS} = 2.5 V and channel length, L = 100 nm.

Fig. 6 shows the variation of subthreshold current for different substrate biases. It is observed that the subthreshold current decreases with increasing substrate bias in the negative direction. The results are in consistent with the substrate bias effect on subthreshold current found in the literature. But it has also been observed that the amount of current increment is less, and the subthreshold slope decreases more rapidly as the gate voltage increases in the shorter channel length device.

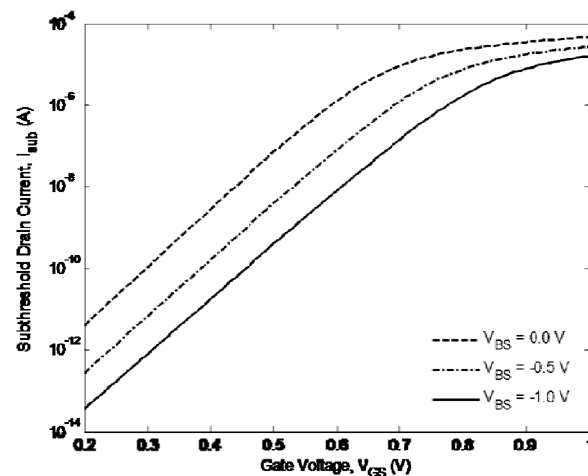

Fig. 6 Subthreshold drain current versus gate voltage for different substrate biases, drain bias, V_{DS} = 0.1 V and channel length, L = 100 nm.

5. CONCLUSIONS

An analytical subthreshold drain current model for ultra thin oxide and nano scale pocket implanted n-MOSFET has been developed based on the conventional drift-diffusion equation and using the surface potential as well as the threshold voltage models for the pocket implanted n-MOSFETs incorporating the effects of substrate and drain bias dependencies. The model is developed assuming two linear pocket profiles along the channel at

the surface of the device from the source and drain edges. The effect of changing the device and pocket profiles parameters on the subthreshold current have been studied using the proposed model. The simulated results show that the proposed model predicts the subthreshold current down to 50 nm channel length. It shows similar behaviour as found in the literature. Hence this model efficiently evaluates the subthreshold drain current of scaled pocket n-MOSFETs having channel lengths in the nano scale regime.

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REFERENCES

[1] S. M. Sze, "Physics of Semiconductor Devices," 2nd Edition, John Wiley and Sons, New York, ch. 8, (1981).

[2] M. Miura-Mattausch, M. Suetake, H. J. Mattausch, S. Kumashiro, N. Shigyo, S. Oganaka and N. Nakayama, "Physical modeling of the reverse short channel effect for circuit simulation," IEEE Transaction on Electron Devices, vol. 48, pp. 2449-2452, Oct. (2001).

[3] M. Orlowski, C. Mazure and F. Lau, "Submicron short channel effects due to gate reoxidation induced lateral interstitial diffusion," IEEE IEDM Technical Digest, p. 632, (1987).

[4] M. Nishida and H. Onodera, "An anomalous increase of threshold voltage with shortening the channel lengths for deeply boron-implanted n-channel MOSFETs," IEEE Trans. on Electron Devices, vol. 48, pp. 1101, (1981).

[5] K. Y. Lim and X. Zhou, "Modeling of Threshold Voltage with Non-uniform Substrate Doping," in Proc. of the IEEE Int'l Conf. on Semiconductor Electronics (ICSE'98), Malaysia, pp. 27-31, (1998).

[6] B. Yu, C. H. Wann, E. D. Nowak, K. Noda and C. Hu, "Short Channel Effect improved by lateral channel engineering in deep-submicrometer MOSFETs," IEEE Transactions on Electron Devices, vol. 44, pp. 627-633, Apr. (1997).

[7] B. Yu, H. Wang, O. Millic, Q. Xiang, W. Wang, J. X. An and M. R. Lin, "50 nm gate length CMOS transistor with super-halo: Design, process and reliability," IEDM Technical Digest, pp. 653-656, (1999).

[8] K. M. Cao, W. Liu, X. Jin, K. Vasant, K. Green, J. Krick, T. Vrotsos and C. Hu, "Modeling of pocket implanted MOSFETs for anomalous analog behavior," IEEE IEDM Technical Digest, pp. 171-174, (1999).

[9] Y. S. Pang and J. R. Brews, "Models for subthreshold and above subthreshold currents in 0.1 μm pocket n-MOSFETs for low voltage applications," IEEE Transactions on Electron Devices, vol. 49, pp. 832-839, May (2002).

[10] J. Tanaka, S. Kimura, H. Noda, T. Toyabe, and S. Ihara, "A sub-0.1 μm grooved gate MOSFET with high immunity to short channel effects," IEEE IEDM Technical Digest, p. 537, (1993).

[11] T. N. Buti, S. Ogura, N. Rovedo, K. Tobimatsu, and C. F. Codella, "Asymmetrical halo source GOLD drain (HS-GOLD) deep-half-micron n-MOSFET design for reliability and performance," IEEE IEDM Technical Digest, pp. 617, (1989).

[12] A. Chatterjee, J. Liu, P. K. Mozumder, M. Rodder and I. C. Chen, "Pass transistor designs using pocket implant to improve manufacturability for 256-Mbit DRAM and beyond," IEEE IEDM Technical Digest, p. 87, (1994).

[13] H. Chen, J. Zhiao, C. S. Teng, L. Moberly and R. Lahri, "Submicron large-angle-tilt-implanted drain technology for mixed signal applications," IEEE IEDM Technical Digest, p. 91, (1994).

[14] J.-G. Su, C.-T. Huang, S.-C. Wong, C.-C. Cheng, C.-C. Wang, H.-L. Shiang and B.-Y. Tsui, "Tilt angle effect on optimizing HALO PMOS and NMOS performance," in Proc. of IEEE IEDM, pp. 11-14, (1997).

[15] H. S. Shin, C. Lee, S. W. Hwang, B. G. Park and H. S. Min, "Channel length independent subthreshold characteristics in submicron MOSFETs," IEEE Electron Device Letters, vol. 19, pp. 137-139, Apr. (1998).

[16] C. S. Ho, J. J. Liou, K.-Y. Huang and C.-C. Cheng, "An analytical subthreshold current model for pocket implanted NMOSFETs," IEEE Trans. On Electron Devices, vol. 50, pp. 1475-1479, Jun. (2003).

[17] M. H. Bhuyan and Q. D. M. Khosru, "Linear Profile Based Analytical Surface Potential Model for Pocket Implanted Sub-100 nm n-MOSFET," Journal of Electron Devices, ISSN 1682-3427, vol. 7, pp 235-240, (2010).

[18] T. A. Fieldly and M. Shur, "Threshold voltage modeling and the subthreshold operation of short-channel MOSFETs," IEEE Transactions on Electron Devices, vol. 40, pp. 137, Jan. (1993).

[19] M. H. Bhuyan and Q. D. M. Khosru, "Linear Pocket Profile Based Threshold Voltage Model for Sub-100 nm n-MOSFET Incorporating Substrate and Drain Bias Effects," in Proc. of the 5th International Conference on Electrical and Computer Engineering (ICECE 2008), Dhaka, pp. 447-451, December 20-22, (2008).