Journal of Electron Devices, Vol. 13, 2012, pp. 910-919

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Journal of Electron Devices
www.jeldev.org

DAA, POTENTIAL DISTRIBUTION AND CARRIER TRANSPORT PHENOMENA OF G^4-FET: A COMPREHENSIVE STUDY

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Received 15-01-2012, online 07-02-2012

ABSTRACT

The G^4-FET features unchallenged functional flexibility originated from the independent biasing of the four gates. It enables compact circuit designs and direct comparison between surface and bulk conduction properties. This paper presents comprehensive studies of the G^4-FET. The physics of depletion all around (DAA) operation, potential distribution and transport phenomena are the objectives of this contribution. This work also tried to incorporate both qualitative and quantitative results of this device available in the published literatures.

Keywords: G4-FET, DAA, transconductance, mobility.

I. INTRODUCTION

The G^4-FET combines an accumulation-mode SOIMOSFET and a lateral double-gate JFET in a single transistor. The G^4-FET is an innovative silicon-on-insulator (SOI) transistor with maximum functional flexibility. It consists of a channel surrounded by four gates with independent biases.

Due to its multiple independent gates, the use of the G^4-FET enhances circuit design flexibility while reducing transistor count as compared to standard CMOS implementations [1]. Depletion all around (DAA) operation is more versatile than that of a JFET because the use of the extra MOS gates results in superior electrical characteristics. In addition, the DAA operation benefits from the high-density integration advantage enabled by the SOI CMOS technology, which is not available in bulk JFET technology.

II. DEVICE STRUCTURE AND OPERATION

The n-channel G^4-FET is actually a p-channel SOIMOSFET with the two body contacts on each side of the channel (Fig. 1). In G^4-FET, the body contacts of the p-MOSFET are used as the source and drain. Drain–current, which is comprised of majority carriers, flows in the direction perpendicular to that of the p-MOSFET current (Fig. 1). The source and drain of the p-MOSFET are used as two extra gates in G4-FET: The lateral junction–gates JG1 and JG2 are reverse biased with respect to the channel and provide JFET-like control on the drain–current. The G4-FET can basically be seen as an “accumulation-mode MOSFET featuring two junction–gates” or reciprocally, as a “JFET provided with two MOS gates.” The front gate G1 induces accumulation when the G^4-FET operates in accumulation mode and induces depletion or inversion when the G^4-FET operates in buried-channel (volume conduction) mode. The substrate emulates a back gate G2, and its action is similar to that of G1.

The G^4-FET provides an ultimate functional flexibility owing to the fact that G1, G2, JG1, and JG2 can be independently biased. When the G^4-FET is used like an accumulation-mode MOSFET, it is driven by the front gate G1, and the drain–current is due to the carriersaccumulated at the front surface via V_{G1} because full depletion (FD) at $V_{G1} = 0$ V can be achieved by adjusting the reverse bias on the junction–gates [1,2]. When the body is FD, its potential distribution becomes a function of the bias on the four gates. The threshold voltage $V_{T,G1}$, which is defined as the V_{G1} bias leading to the onset of the front-surface accumulation current, depends on $V_{JG1,2}$ and V_{G2}.

In JFET-like operation, the G^4-FET enables a volume current to be controlled by the junction–gates. In that case, the static parameters related to the junction–gates depend on V_{G1} and V_{G2} through the corresponding surface potentials.

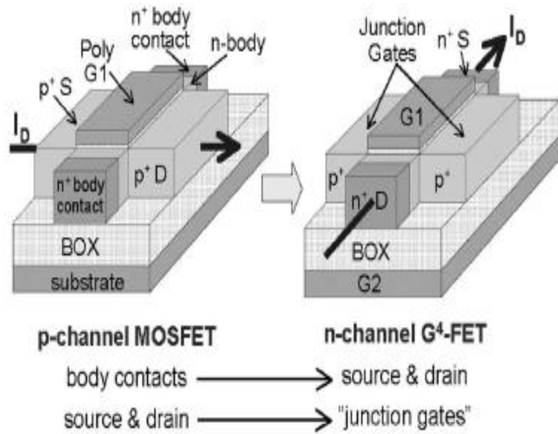


Figure 1. N-channel G^4-FET structure and its equivalence to a p-channel MOSFET with the two body contacts.

II.1 Depletion all around (DAA) operation

When all four gates of an n-channel G^4-FET are appropriately biased, DAA operation is obtained, inducing depletion at both silicon/oxide and n-silicon/ p+ junction interfaces. In DAA operation, the G^4-FET is driven by the junction gates that are interconnected ($V_{JG1} = V_{JG2} = V_{JG}$). The front and back MOS gates are biased to constant voltages, inducing either depletion or inversion at the silicon/oxide interfaces. Consequently, I_D flows at the center of the silicon film, and the conducting channel is surrounded by depletion regions.

There are three possible combinations for the DAA mode with respect to silicon/oxide interface conditions (see Fig. 2) [2]:

1) Both interfaces are in depletion.
2) One interface is in depletion, while the other is in inversion.
3) Both interfaces are in inversion.

The device performance and properties in DAA mode are remarkably affected by the presence of inversion layers.

The three combinations illustrated in Fig. 2 for an n-channel G^4-FET can be achieved by applying the appropriate front- and back gate voltages. In the first combination (A), where both interfaces are in depletion, the channel is pinched off in the lateral direction for $V_{JG} \geq V_{T,JG}$. For VJG < $V_{T,JG}$, the lateral depletion regions shrink, and a conducting channel appears and gradually widens, resulting in an increase in drain–current. A gradual decrease in $V_{T,JG}$ and, consequently, in the maximum drain–current (obtained for $V_{JG} = 0$) is observed when the front interface (B) or both interfaces (C) are driven from depletion to inversion.

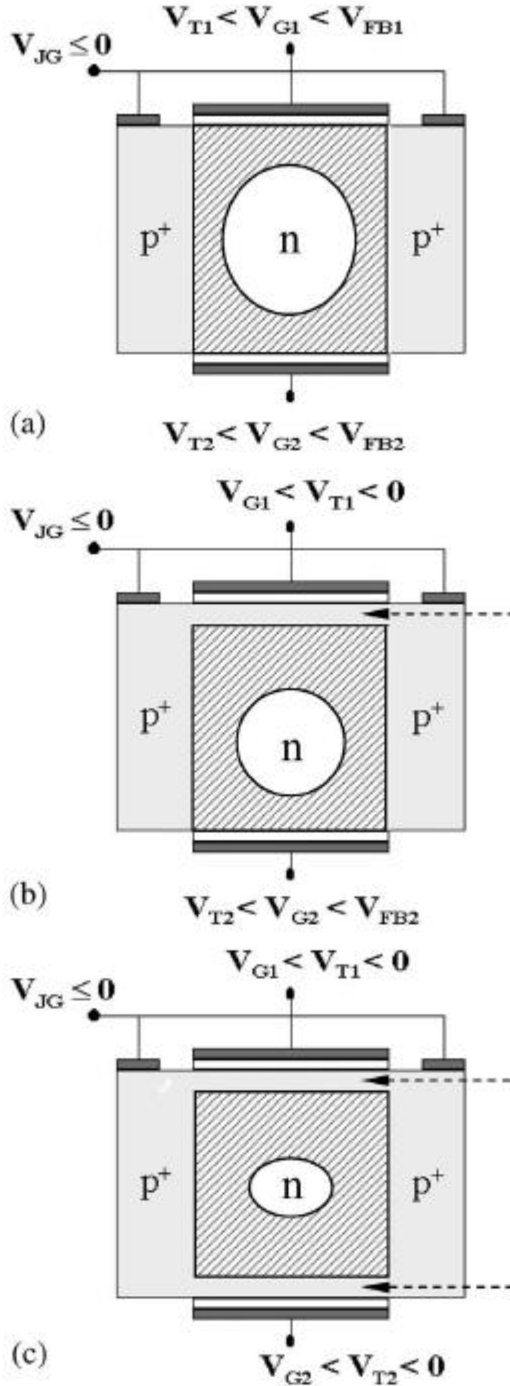


Figure 2. Different combinations of the DAA conduction for an n-channel G4-FET [8]. (a) Both interfaces depleted. (b) Front interface in inversion and back interface depleted. (c) Both interfaces in inversion. The drain–current flows perpendicular to the figures and the hatched areas represent the depletion regions. $V_{T1,2}$ and $V_{FB1,2}$ designate the inversion threshold and flat-band voltages associated to front/back gates, respectively.

III. ELECTROSTATIC POTENTIAL DISTRIBUTION

The device considered here is an n-channel G4-FET, with the source grounded and the drain at a voltage V_D. Front-gate voltage (V_{G1}), back-gate voltage (V_{G2}) and junction-gate voltages ($V_{JG1,2}$) are such that the channel is fully-depleted. Along the channel, potential gradually increases from zero at source to V_D at drain. It can be assumed that this variation is parabolic due to MOS gates. This assumption is usually made in dealing with short channel effects [1]. The body potential can be expressed with respect to the source as

$$\psi(x, y, z) = a(x, y)z^2 + b(x, y)z + c(x, y) \quad [1]$$

The coefficients of Eqn. (1) can be evaluated using the following boundary conditions (see fig. 3)

$$\psi\left(x, y, -\frac{L}{2}\right) = 0 \quad and \quad \psi\left(x, y, \frac{L}{2}\right) = V_D \quad [2]$$

The evaluated coefficients are

$$c(x, y) = \psi(x, y, 0);\ b(x, y) = \frac{V_D}{L} \quad and \quad [3]$$
$$a(x, y) = \frac{2V_D - 4\psi(x, y, 0)}{L^2}$$

Substituting Eqn. (3) into Eqn. (1), body potential yields

$$\psi(x, y, z) = \psi(x, y, 0)\left(1 - \frac{4z^2}{L^2}\right) + \frac{2V_D}{L^2}z^2 + \frac{V_D}{L}z \quad [4]$$

Using full-depletion approximation, 3-D Poisson's equation can be written as

$$\frac{\partial^2\psi(x, y, z)}{\partial x^2} + \frac{\partial^2\psi(x, y, z)}{\partial y^2} + \frac{\partial^2\psi(x, y, z)}{\partial z^2} = -\frac{qN_D}{\varepsilon_{Si}} \quad [5]$$

The solution of Eqn. (5) can be readily attained by transforming it first into 2-D and then into 1-D partial differential equation.

Substituting Eqn. (4) into Eqn. (5) and then evaluating it at z = 0 yields 2-D Poisson's equation and then evaluating it at x = 0 yields 1-D Poisson's equation

$$\frac{\partial^2\psi(x,y,0)}{\partial x^2}+\frac{\partial^2\psi(x,y,0)}{\partial y^2}-\frac{8}{L^2}\psi(x,y,0)+\frac{4V_D}{L^2}=-\frac{qN_D}{\varepsilon_{Si}}\quad for\quad (2-D);$$

$$and$$

$$\frac{d^2\psi(0,y,0)}{dy^2}-8\left(\frac{1}{W^2}+\frac{1}{L^2}\right)\psi(0,y,0)+\frac{8}{W^2}\left\{\frac{V_{JG1}+V_{JG2}}{2}-\left(\frac{E_g}{q}+\frac{kT}{q}\ln\frac{N_D}{n_i}\right)\right\}+\frac{4V_D}{L^2}=-\frac{qN_D}{\varepsilon_{Si}}\quad for\quad (1-D) \qquad [6]$$

where L = channel length, N_D = doping concentration of channel and W = channel width..

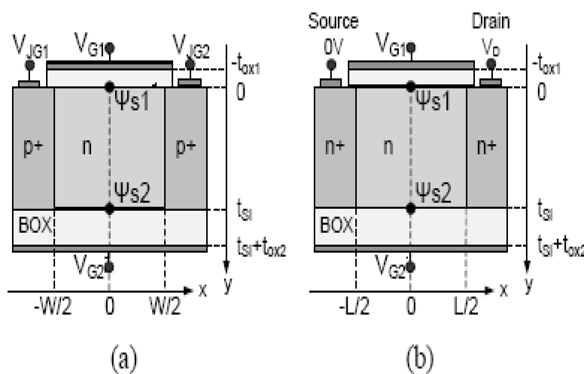


Figure 3. Cross sections of n-channel G^4-FET showing the axes and necessary symbols. The drain-current flow direction is (a) perpendicular to the figure. (b) from right to left of the figure.

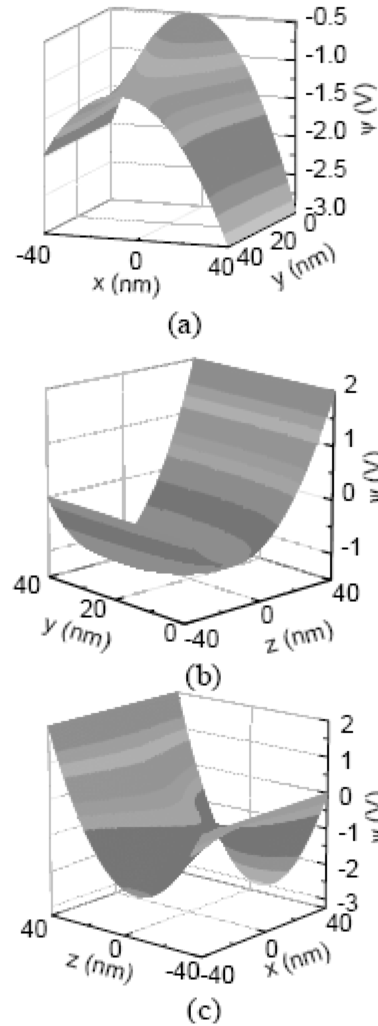


Figure 4 3-D plot of potential distribution in the body of an n-channel G^4-FET. Potential distribution in (a) z = 0 plane. (b) x = 0 plane. (c) y = 0 plane. Structural parameters: W = 80nm, L = 5μm, t_{si} = 40nm, t_{ox1} = 5nm, t_{ox2} = 50nm, $N_D=10^{17}cm^{-3}$. Bias conditions: V_{G1}=0.5V, V_{G2}=5V, V_{JG1}=-1V, V_{JG2}=-2V and V_D=2V.

Using appropriate boundary conditions, both 2-D and 1-D Poisson's equations can be solved for $\psi(x,y,0)$ and $\psi(0,y,0)$. Substituting these values in Eqn. (4) will yield the overall potential expression of $\psi(x,y,z)$. The complete expression of $\psi(x,y,z)$ is given in appendix A.

III.1 C-V Characteristics

In reference to Fig.3 and Fig.4, when equal junction voltages are applied i.e. V_{JG1} = V_{JG2} the local surface potentials

$\psi(0,0,0)$ at y = 0 and $\psi(0,t_{Si},0)$ at y = t_{Si} corresponds to maximum. But when junction voltages are not equal, it is convenient to express the surface potentials as peak surface potentials which are given by [3]

$$\psi_m(y) = -\frac{\left(V_{JG2}-V_{JG1}\right)^2}{16\left[\left\{\frac{V_{JG1}+V_{JG2}}{2}-\left(\frac{E_g}{q}+\frac{kT}{q}\ln\frac{N_D}{n_i}\right)\right\} - \psi(0,y,0)\right]} + \psi(0,y,0) \quad [7]$$

Setting y = 0 and y = $t_{Si,}$ peak surface potentials can be evaluated as

$$\psi_m(y)\Big|_{y=0} = \psi(0,0,0) = \psi_{m1} \quad [8]$$

and,

$$\psi_m(y)\Big|_{y=t_{Si}} = \psi(0,y,0) = \psi_{m2} \quad [9]$$

Peak surface potentials can also be evaluated using the relation of contact potential with surface with peak surface potential and potential drop across oxide layer, for example, for front gate peak surface potential

$$\psi_{m1} = V_{G1} - \left(V_{ox1} + \phi_{ms1}\right) \quad [10]$$

Similarly back gate peak surface potential

$$\psi_{m2} = V_{G2} - \left(V_{ox2} + \phi_{ms2}\right) \quad [11]$$

where,

$\phi_{ms1,2}$ = work function difference between the silicon and front/back-gate material.

$$V_{ox1,2} = \frac{\varepsilon_{Si}E_{m1,2} - Q_{ox1,2}}{C_{ox1,2}} = \frac{\varepsilon_{Si}E_{m1,2} - Q_{ox1,2}}{\frac{\varepsilon_{ox}}{t_{ox1,2}}} \quad [12]$$

$C_{ox1,2}$ = front/back-gate oxide capacitance

$$E_{m1,2} = -\frac{d\psi_m(y)}{dy}\Big|_{y=0,t_{Si}} \quad [13]$$

Combining Eqn. (10)-(13), the expression for the front-gate contact potential V_{G1} and back-gate contact potential V_{G2} as a function of gate capacitances can be obtained. The complete expression for V_{G1} and V_{G2} can be found in appendix *B*.

III.2 Carrier concentration

Majority carrier (in this case electron for n channel) concentration for non-equilibrium condition can be calculated as [14]

$$n(x,y,z) = n_0 e^{\frac{\psi(x,y,z)}{\frac{kT}{q}\ln\frac{N_D}{n_i}}} \quad [14]$$

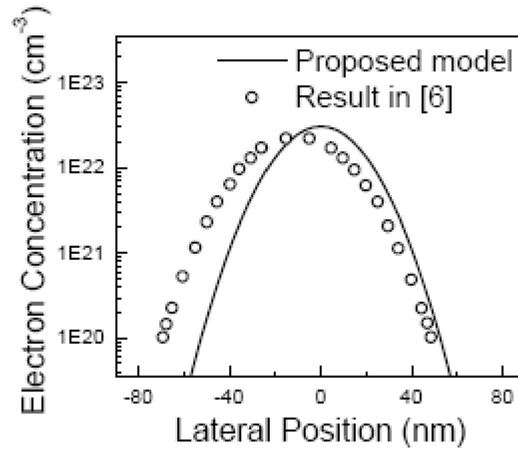


Figure 5. Electron concentration as a function of the lateral position, at the middle length of the channel and at 80nm from top surface, for V_{JG1} = V_{JG2} = -0.7V. Structural parameters: W=0.35µm, L=3.4µm, t_{si}=150nm, t_{ox1}=8nm, t_{ox2}=350nm. Bias conditions: V_{G1}=0V, V_{G2}=-9.5V, V_D=50mV.

IV. TRANSPORT CHARACTERISTICS

IV.1 I-V characteristics

Expressing the drain-current as a function of terminal voltage, the cross section of an n-channel G4-FET shown in fig. 6 is considered related to the DAA mode.

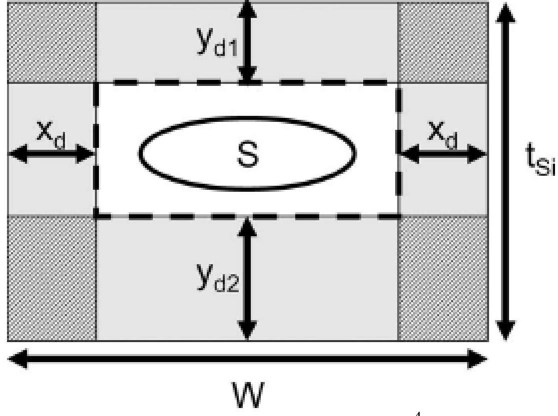


Figure. 6. Cross section of the G4-FET body perpendicular to current flow direction, showing the symbols used in dc modeling (V_{JG1} = V_{JG2} = V_{JG}). The dashed rectangle shows the channel cross section in case the charge sharing between the vertical and lateral depletion regions has not been taken into account. The solid ellipsoid represents the actual shape of the channel cross section, with charge sharing included.

When the depletion widths are comparable to device width and height, 3-D simulations suggest that the sectional shape of the conducting channel is closer to an ellipse than a rectangle [3].

The drain-current in DAA mode is expressed as

$$I_D = \frac{q\mu_n N_D}{L}\int_0^{V_D} S(V)dv \qquad [15]$$

where

$$S(V) = (W - 2x_d)(t_{Si} - y_{d1} - y_{d2}) - 2\alpha x_d(y_{d1} + y_{d2}) \qquad [16]$$

Here,

$$x_d = \sqrt{\frac{2\varepsilon_{Si}(V - V_{JG} + \frac{kT}{q}\ln\frac{N_D}{n_i})}{qN_D}} \qquad [17]$$

$$y_{d1} = \left(\frac{\varepsilon_{Si}}{C_{ox1,2}}\right)\left[-1 + \sqrt{1 + \frac{2C_{ox1,2}^2(V - V_{G1,2} + V_{FB1,2})}{qN_D\varepsilon_{Si}}}\right] \qquad [18]$$

$$y_{d2} = \sqrt{\frac{2\varepsilon_{Si}(V - V_{JG} - 2\Phi_F)}{qN_D}} \qquad [19]$$

Analytical solutions are possible for every combination of DAA described in Fig. 2. Here the case (c) in fig.2 is considered to derive the analytical expression for drain-current because this case provides the highest device performance. When both interfaces are in inversion, combining Eqn. (15)-(19), the drain-current in the nonsaturation region can be expressed (see appendix C for complete expression).

The drain-current for saturation region can be obtained replacing V_D by V_{Dsat}. The threshold (pinchoff) and saturation voltages are given by the condition $S=0$ (remember for inversion condition, $x_d=y_{d1,2}$) at the source and drain side, respectively. If we solve (16) for $S = 0$ and then evaluate it for $x_d\big|_{V=V_D}$, it will yield the expression for V_{Dsat} as [4]

$$V_{Dsat} = V_{JG} - \frac{kT}{q}\ln\frac{N_D}{n_i} - \frac{qN_D}{8\varepsilon_{Si}} \times \left[\frac{(W + t_{Si}) - \sqrt{(W - t_{Si})^2 + 4\alpha W t_{Si}}}{4(1-\alpha)}\right]^2 = V_{JG} - V_{T,JG} \qquad [20]$$

where $V_{T,JG}$ is threshold voltage.

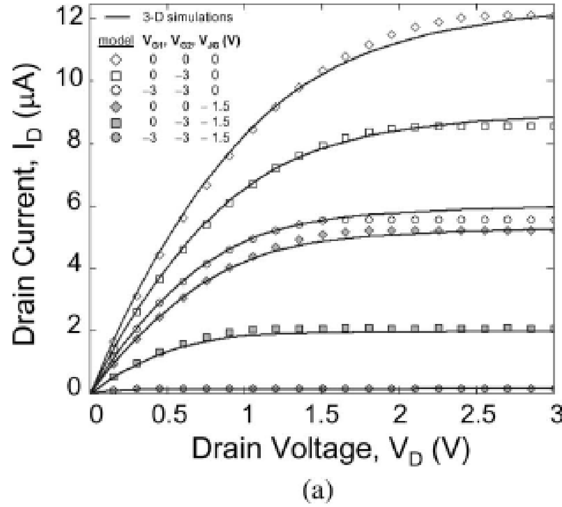
IV.2 Transconductance, Carrier mobility

The carrier mobility in the volume channel can be estimated by biasing both interfaces at flat-band: $V_{G1} = V_{FB1}$ and $V_{G2} = V_{FB2}$. For a low drain voltage, the drain–current and transconductance of an n-channel G4-FET operating above threshold are then simply given by[5]

$$I_D = \frac{q\mu_n N_D t_{Si} W}{L} \times \left[1 - 2\sqrt{\frac{2\varepsilon_{Si}}{qN_D W^2}}\left(\frac{kT}{q}\ln\frac{N_D}{n_i} - V_{JG}\right)V_D\right] \qquad [21]$$

and,

$$\frac{\partial I_D}{\partial V_{JG}} = g_m = V_D \frac{t_{Si}}{L} \sqrt{\frac{2\varepsilon_{Si} q N_D}{\frac{kT}{q}\ln\frac{N_D}{n_i} - V_{JG}}} \qquad [22]$$



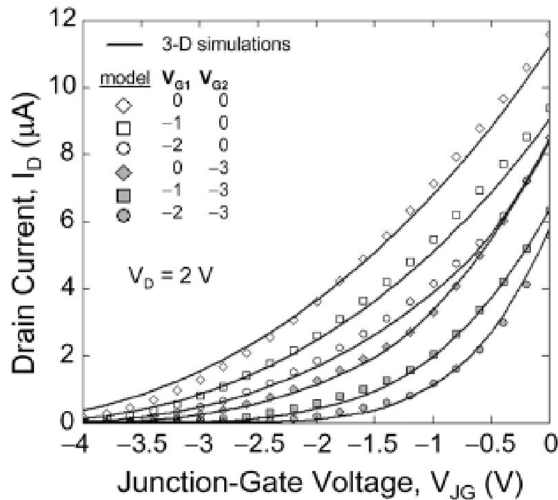


Figure 7. Calculated versus simulated drain–current of an n-channel G4-FET (a) as a function of the drain voltage and (b) as a function of the junctiongate voltage for V_D = 2 V. α= 0.105, W = 250 nm, L = 5 μm, t_{Si} = 200 nm, $t_{\text{ox1}} = t_{\text{ox2}}$ = 10 nm, $\phi_{\text{m1,2}}$ = 5.25 eV and N_D = 5 .10^{1}7 cm^{-3} implying μ_n = 360 cm^2/V.s.

Carrier mobility can be derived by eliminating N_D from Eqn. (21) and Eqn. (22)

$$\mu_n = \frac{g_m W L}{2\varepsilon_{Si} t_{Si} V_D \left(\frac{I_D}{g_m \left(\frac{kT}{q}\ln\frac{N_D}{n_i} - V_{JG} \right)} + 2 \right)} \qquad [23]$$

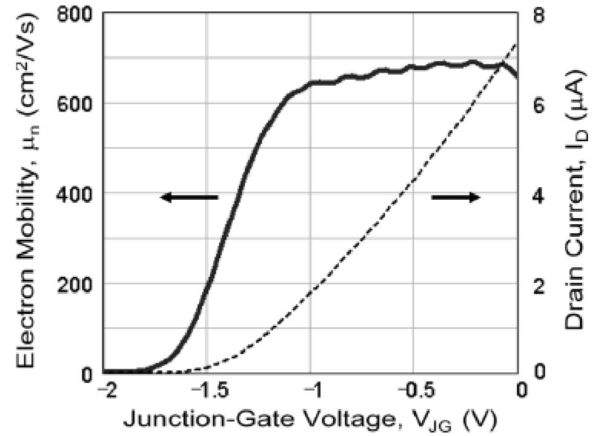


Figure 8. Measured electron mobility as a function of the junction-gate bias for an n-channel G4-FET ($V_{\text{G1}} = V_{\text{FB1}}$ = 0.33 V and $V_{\text{G2}} = V_{\text{FB2}}$ = 0 V).

The variation of the electron mobility μ_n in an n-channel G4-FET extracted from the measurement by using Eqn. (23) is shown in Fig. 8 as a function of the junction-gate voltage. Above threshold ($V_{\text{JG}} > -1.2$ V), (23) provides a quasi-constant mobility (~650 cm^2/s at 300 K). This value corresponds to the mobility limited by ionized impurity scattering (including acoustic phonon scattering) for $N_D \cong 1.5\times10^{17}\text{cm}^{-3}$. This means that DAA mode yields a bias-independent bulk mobility determined essentially by the doping density. Particularly, when interfaces are driven to inversion [case (c) in Fig. 2], the oxide and interface defects are shielded, and their adverse influence (if any) on the volume mobility is prevented. Similar trends are observed for the hole mobility in p-channel G4-FET [6-8].

V. CONCLUSION

The analytical expressions of 3-D electrostatic potential distribution (carrier concentration, C-V characteristics) and transport characteristics (I-V characteristics, transconductance and mobility) of G^4-FET for modeling purpose along with experimental results are presented. A comprehensive study of the G^4-FET would be very important for readers, scientists, and engineers.

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Appendix A.

$$\psi(x,y,z)=\left\{\left[\frac{\frac{V_{JG1}+V_{JG2}}{2}-\frac{kT}{q}\ln\frac{N_D}{n_i}+\frac{qN_DW^2}{8\varepsilon_{Si}}+\frac{W^2}{2L^2}V_D}{1+\frac{W^2}{L^2}}+\frac{(\psi_{m2}-G_2+\frac{W^2V_D}{W^2+L^2})\sinh\beta y+(\psi_{m1}-G1+\frac{W^2V_D}{W^2+L^2})\sinh\beta(t_{Si}-y)}{2\sinh\beta t_{Si}}\right]\times (1-\frac{4x^2}{W^2})+\frac{4x^2}{W^2}\left(\frac{V_{JG1}+V_{JG2}}{2}-\frac{kT}{q}\ln\frac{N_D}{n_i}\right)+\frac{V_{JG2}-V_{JG1}}{W}x\right\}\times \left(1-\frac{4z^2}{L^2}\right)+\frac{2V_D}{L^2}z^2+\frac{V_D}{L}z$$

Where

$$G_{1,2}=\frac{1-\frac{W^2}{L^2}}{1+\frac{W^2}{L^2}}\left(\frac{V_{JG1}+V_{JG2}}{2}-\frac{kT}{q}\ln\frac{N_D}{n_i}\right)-\sqrt{\left[\left(\psi_{m1,2}-V_{JG1}+\frac{kT}{q}\ln\frac{N_D}{n_i}\right)\left(\psi_{m1,2}-V_{JG2}+\frac{kT}{q}\ln\frac{N_D}{n_i}\right)\right]}+\frac{qN_DW^2}{4\varepsilon_{Si}}\frac{W^2}{W^2+L^2}$$

and

$$\beta=\frac{2\sqrt{2}}{W}\sqrt{1+\frac{W^2}{L^2}}$$

Appendix B.

$$V_{G1} = V_{FB1} + \psi_{m1} + \frac{C_{jg}}{2C_{ox1}} \left\{ 1 - \frac{\left(V_{JG2} - V_{JG1}\right)^2}{4\left(\frac{V_{JG1} + V_{JG2}}{2} - \frac{kT}{q}\ln\frac{N_D}{n_i} - \psi_{m1} - \sqrt{\left(\psi_{m1} - V_{JG1} + \frac{kT}{q}\ln\frac{N_D}{n_i}\right)\left(\psi_{m1} - V_{JG2} + \frac{kT}{q}\ln\frac{N_D}{n_i}\right)} \right)^2} \right\}$$

$$\times \left[\frac{\beta W}{\tanh \beta t_{Si}}\left(\psi_{m1} - G_1\right) - \frac{\beta W}{\sinh \beta t_{Si}}\left(\psi_{m2} - G_2\right) - \left(\frac{\beta W}{\sinh \beta t_{Si}} - \frac{\beta W}{\tanh \beta t_{Si}} \right) \frac{W^2 V_D}{W^2 + L^2} \right]$$

$$V_{G2} = V_{FB2} + \psi_{m2} + \frac{C_{jg}}{2C_{ox2}} \left\{ 1 - \frac{\left(V_{JG2} - V_{JG1}\right)^2}{4\left(\frac{V_{JG1} + V_{JG2}}{2} - \frac{kT}{q}\ln\frac{N_D}{n_i} - \psi_{m2} - \sqrt{\left(\psi_{m2} - V_{JG1} + \frac{kT}{q}\ln\frac{N_D}{n_i}\right)\left(\psi_{m2} - V_{JG2} + \frac{kT}{q}\ln\frac{N_D}{n_i}\right)} \right)^2} \right\}$$

$$\times \left[\frac{\beta W}{\tanh \beta t_{Si}}\left(\psi_{m2} - G_2\right) - \frac{\beta W}{\sinh \beta t_{Si}}\left(\psi_{m1} - G_1\right) - \left(\frac{\beta W}{\sinh \beta t_{Si}} - \frac{\beta W}{\tanh \beta t_{Si}} \right) \frac{W^2 V_D}{W^2 + L^2} \right]$$

Appendix C.

$$I_D = \frac{q\mu_n N_D}{L} \left\{ \begin{matrix} (1-\alpha)\frac{8\varepsilon_{Si}}{qN_D}\left[\begin{matrix} (\frac{kT}{q}\ln\frac{N_D}{n_i} - \\ V_{JG})V_D + \frac{V_D^2}{2} \end{matrix} \right] - \frac{4}{3}(W + t_{Si}) \times \sqrt{\frac{2\varepsilon_{Si}}{qN_D}\left[(\frac{kT}{q}\ln\frac{N}{n_i} - V_{JG} + V_D)^{\frac{3}{2}} - (\frac{kT}{q}\ln\frac{N}{n_i} - V_{JG})^{\frac{3}{2}} \right]} + \\ Wt_{Si}V_D \end{matrix} \right\}$$